Instituto Tecnológico de Tuxtla Gutiérrez

Ingeniería Electrónica

Reporte de Residencia Profesional.
Complementación e Implementación de un Transmisor-Receptor FSK Vía Inalámbrica

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INTRODUCCIÓN.

La propagación de señales a través de medios de transmisión es dependiente de las características especificas de dicho medio, de ahí que sea necesario adecuar las señales de información al transmitir por el canal de comunicaciones que será utilizado como medio de transmisión. Este proceso de adaptación de las señales de información al medio que se va transmitir es lo que se conoce como Modulación de la Señal.

En el extremo contrario, en la recepción, será necesario hacer la operación contraria, es decir, recuperar la señal de información a partir de la señal modulada. Este proceso se conoce como proceso de Demodulación de la Señal. El proceso de modulación y demodulación de la señal permite la transmisión de señales a través del canal de comunicaciones de forma eficiente. Este proceso de modulación consiste en un desplazamiento de la banda base de la señal de información hacia frecuencias más altas que resultan más adecuadas para la transmisión, y en el proceso de recepción se requiere el correspondiente desplazamiento a la banda original para la recuperación de la señal de información.

La radio digital es la transmisión y la recepción de sonido que ha sido procesado utilizando una tecnología comparable a la que se usa en los reproductores de discos compactos. En síntesis, un transmisor de radio digital convierte sonidos en series de números o dígitos, es decir, cuando la información sonora se traduce al lenguaje binario de unos y ceros, de ahí el término “radio digital”. En cambio las radios analógicas tradicionales convierten los sonidos en series de señales eléctricas que se asemejan a ondas de sonido.

JUSTIFICACIÓN.

La comunicación a distancia por medio de FSK es importante debido a que en ocasiones las estaciones repetidoras no pueden comunicarse entre sí por medios inalámbricos, por la ubicación geográfica en que se encuentran cada una de ellas.

Debido a estos problemas con la comunicación entre estaciones repetidoras se ha optado por la utilización de comunicación por medio de líneas telefónicas para optimizar la comunicación entre estaciones y dar un mejor servicio.

El proyecto brinda una opción más de transmisión y asegurará la transmisión de programas en vivo con buena calidad de audio en lugares con línea telefónica, ofreciendo un gran ancho de banda para poder llevar la suficiente información en tiempo y forma, cubriendo las necesidades tanto de la empresa como del auditorio radioescucha.

La importancia de realizar este proyecto radica en los beneficios que nos proporciona el convertir una señal analógica en digital, por ejemplo:

- La radio digital FM es capaz de proporcionar un sonido claro de calidad comparable a la de los Discos Compactos (CD´s). Los receptores digitales proporcionan un sonido significativamente más claro que las radios analógicas convencionales.
- La recepción de la radio digital es más resistente a las interferencias y al ruido, además elimina muchas imperfecciones de la transmisión y recepción de la radio analógica.
- En comparación con la radio analógica tradicional, la radio digital ofrece a los oyentes una serie de ventajas que incluyen mejor calidad de audio, señales más fuertes y nuevos servicios auxiliares, tales como canales múltiples de programación de audio, servicios de audio a petición y funciones interactivas.

OBJETIVO GENERAL.

Aplicar los conocimientos adquiridos en la carrera de Ingeniería Electrónica para implementar un sistema de transmisión de datos aplicando FSK de modo inalámbrico.

OBJETIVO ESPECIFICO.

Transmitir y recibir una señal utilizando comunicación FSK de modo inalámbrico.

PLANTEAMIENTO DEL PROBLEMA.

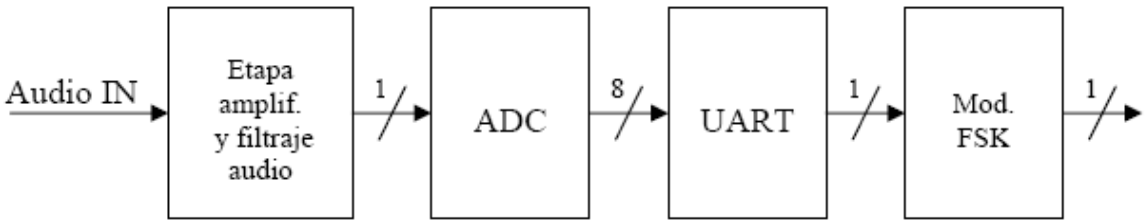
Implementar un dispositivo transmisor que pueda ser usado en cualquier lugar que cuente con una línea telefónica. Las formas de transmisión son diversas, para este caso se ha escogido la modulación por desplazamiento de frecuencia (FSK, por sus siglas en ingles), en la que es necesario digitalizar la señal que será transmitida.

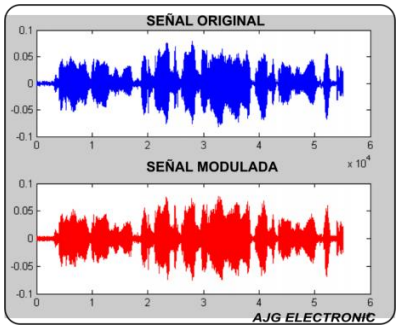
Una vez que se tiene la señal entre el rango de voltaje deseado, se procederá a convertir la señal analógica en una combinación de unos y ceros para que pueda ser transmitida y posteriormente recibirla para convertirla ahora de unos y ceros a una señal analógica (Modulación y Demodulación).

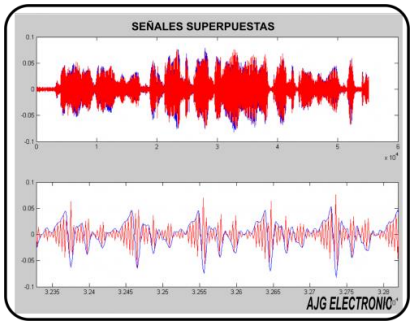
1. Emisor

1.1. Funcionamiento

Es un transmisor completo FSK, desde la entrada de audio a través de un Jack-midi, hasta obtener la señal modulada. El esquema global del transmisor sería el siguiente:







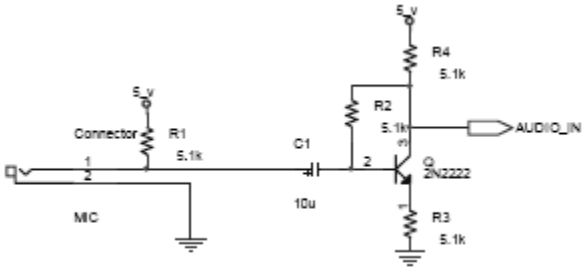
1.2. Partes

Como se ve en el diagrama anterior, en transmisor básicamente consta de 4 partes:

a) Una etapa de audio, filtraje y amplificación.
b) El convertidor analógico – digital.
c) Un Pic que utilizamos como la UART del transmisor.
d) El modulador FSK.

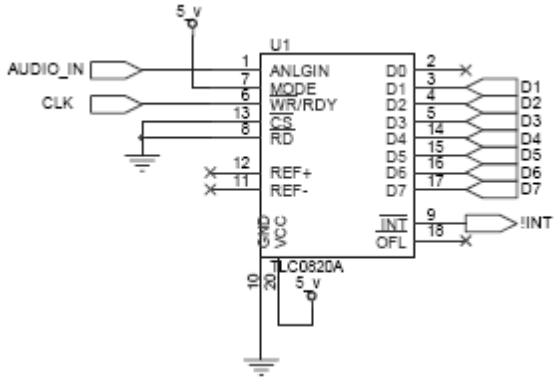
1.2.1. Etapa de audio

La etapa de audio se compone básicamente de un amplificador basado en un transistor q2n2222 polarizado en Clase C para amplificar de forma importante el audio. Se puede incluir un condensador de 1nF del colector a masa con la función de adaptación y filtraje.



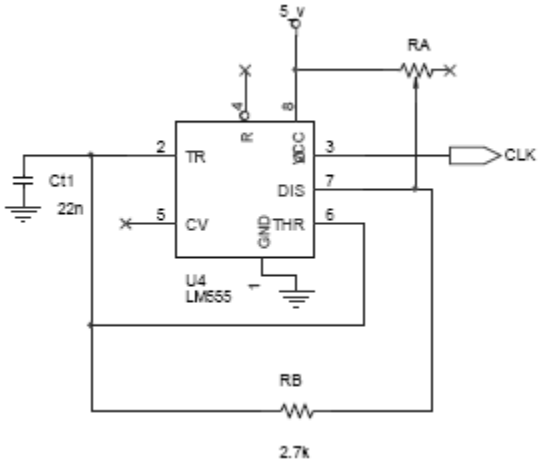
1.2.2. Conversión Analógico – Digital

Como **convertidor** analógico-digital hemos utilizado el chip TLC0820AC, de la marca Texas Instruments, con el que disponemos de una resolución de 8 bits.



Este chip nos es muy útil ya que como se aprecia en el esquema no precisa de componentes externos, salvo de un oscilador que le indica cuando ha de convertir. Esta frecuencia viene dada por una componente de la familia 555, el cual lo hacemos oscilar a una frecuencia fija de 8k, ya que es la frecuencia utilizada para digitalizar la voz, y conseguir una transmisión serie a 64khz.

El esquema de este oscilador es el siguiente:



Para el cálculo de las componentes hemos elegido que la frecuencia de trabajo, como ya hemos comentado, sea de 8khz, y tengamos una relación de estancia en cero el doble que de estancia en 1, es decir que debe permanecer el doble de tiempo en cero que en 1. Con ellos tenemos:

$$f = 8k = \frac{1'44}{(R_A + 2R_B)C}$$

$$t = t_H + t_L = 3t_L = 125\mu \implies t_L = 41'47\mu s$$

$$\left.\begin{array}{l} t_L = 0.693\ R_B\ C = 41'47\mu \\ 125\mu = 0.693\ (R_A + 2R_B)C \end{array}\right\}$$

De aquí elegimos el valor de C=22nF, y que la relación de sumas de resistencia sea 10kΩ, con ello obtenemos unos valores de resistencias:

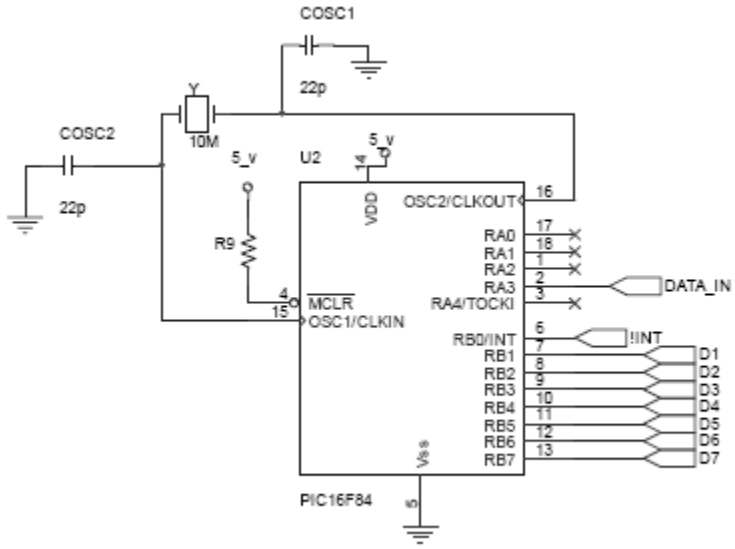
Ra = 4.53kΩ y Rb=2.733kΩ.

Pero para asegurarnos de los valores, fijamos la resistencia Rb a 2.7kΩ y fijamos la primera con un potenciómetro de 10kΩ, para asegurarnos la oscilación a 8khz.

1.2.3. La UART de Transmisión

Una vez los datos están en formato digital, son tratados mediante un microcontrolador PIC16F84. El cual es utilizado para realizar la transmisión serie, la UART. Para ellos tomamos los datos en paralelo que nos llega desde el ADC, y a una velocidad de 67.2khz, una frecuencia próxima a los 64khz que hubiéramos deseado, y que nos permite el PIC conseguir con el cristal de 10Mhz utilizado.

El esquema externo es el siguiente:



La programación de este microcontrolador se realiza en lenguaje C. El código es bastante sencillo, únicamente capturamos en señal por en puerto paralelo (B), y lo enviamos por el pin2 (RA3), perteneciente al puerto B.

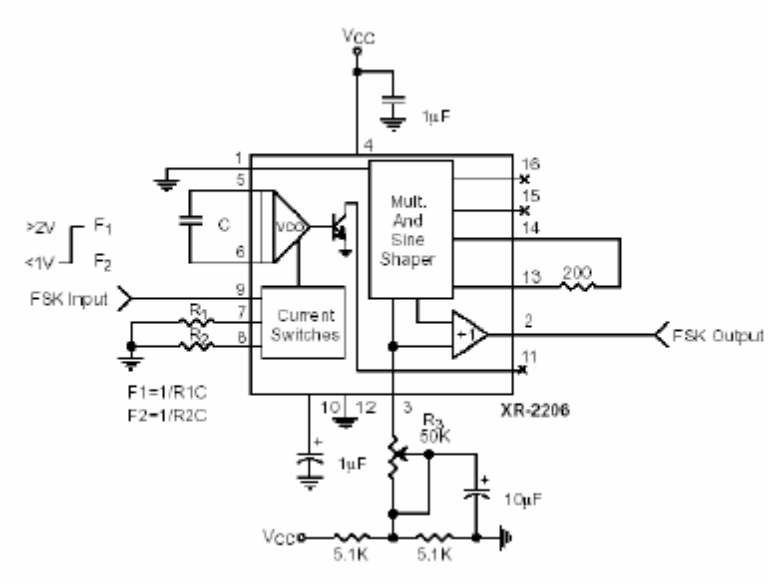
El código de la PIC es el siguiente:

```
#pragma CLOCK_FREQ 10000000
//RS232 settings
#pragma TRUE_RS232 1
#pragma RS232_TXPORT PORTA
#pragma RS232_RXPORT PORTA
#pragma RS232_TXPIN 3
#pragma RS232_RXPIN 4
#pragma RS232_BAUD 67200
#define PUERTO_A 0x10
#define PUERTO_B 0xFF
char data=0xA;
char cont=0;
void interrupt () {
data=input_port_b();
clear_bit( INTCON, INTF );
}
main () {
OPTION_REG = 0xC7;
set_bit( STATUS, RP0 );
set_tris_b( PUERTO_B );
set_tris_a( PUERTO_A );
```

```
clear_bit( STATUS, RP0 );
enable_interrupt( GIE );
enable_interrupt( INTE );
for (cont=0;cont<100;cont++) {
putchar(0xFF);
}
for (;;) {
putchar(data);
}
}
```

1.2.4. El modulador FSK

Como modulador hemos utilizado el chip XR2206 de la marca EXAR, que es un chip que nos puede generar señales sinusoidales, cuadradas o triangulares de alta calidad, de la que podemos especificar la amplitud y la frecuencia de la misma. Esto último lo modificamos mediante dos potenciómetros que nos facilitan el afinamiento de la señal. El chip soporta frecuencia desde 0.01hz hasta 1Mhz, por tanto está dentro de nuestra frecuencia de trabajo, que serán 67.2khz para la frecuencia baja y 100khz para la frecuencia alta.

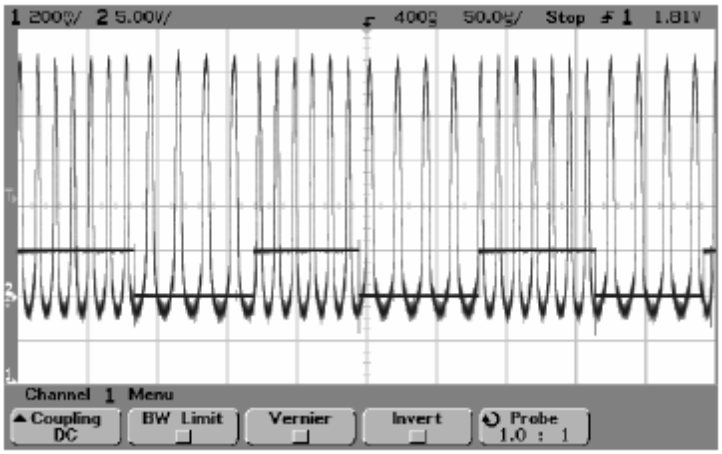


El esquema interno de nuestro chip es el siguiente, donde la amplitud de nuestra señal de salida viene dada por el potenciómetro R3 del pin 3, y las dos frecuencias de oscilación son debidas a las resistencias R1 y R2 de los pines 7 y 8 respectivamente, y del condensador C.

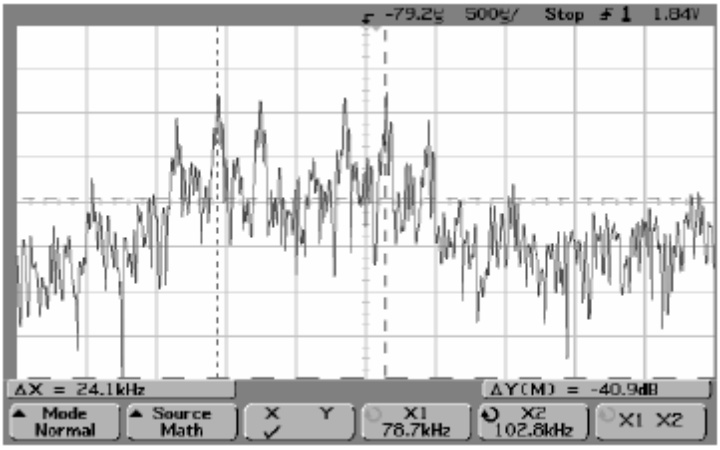
La relación viene dada por f1 = 1/R1C y f2 = 1/R2C, una para la transmisión de los 0 y otra para la de los 1.

Para el cálculo hemos fijado el condensador C=1nF y hemos calculado las R, para las resistencias anteriormente comentadas. Como constante que hemos seguido a lo largo de la práctica, hemos fijado una, y en la otra hemos puesto un potenciómetro para posibles ajustes que pudiéramos necesitar, y afinar más en el valor final.

Podemos ver las señales a su salida:



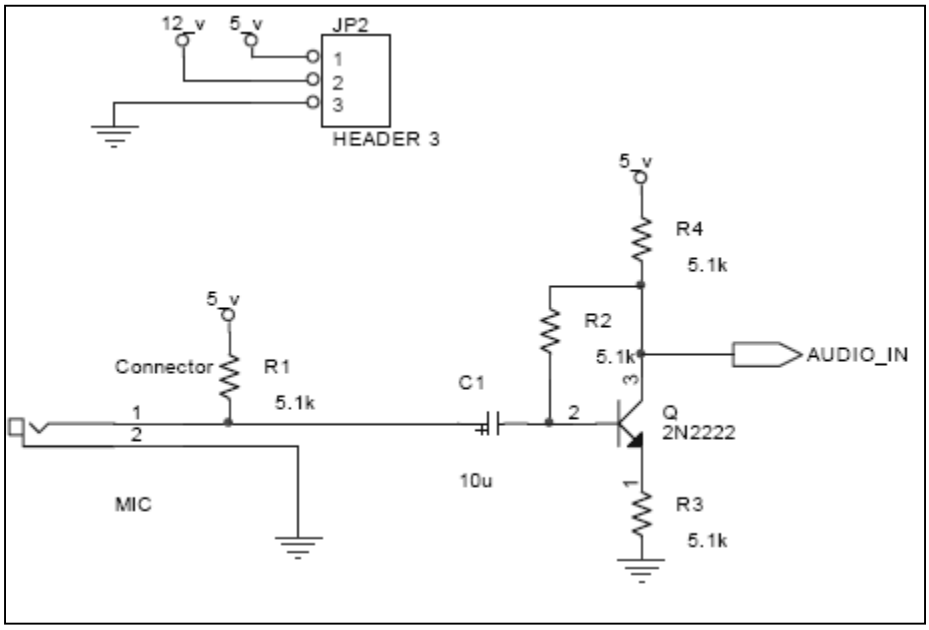
Como podemos observar el modulador varia la frecuencia según si transmitimos un “1” o un “0”. De todas formas ésta no es una señal sinusoidal perfecta. Por tanto en la representación frecuencial no veremos las dos frecuencias claramente diferenciadas.



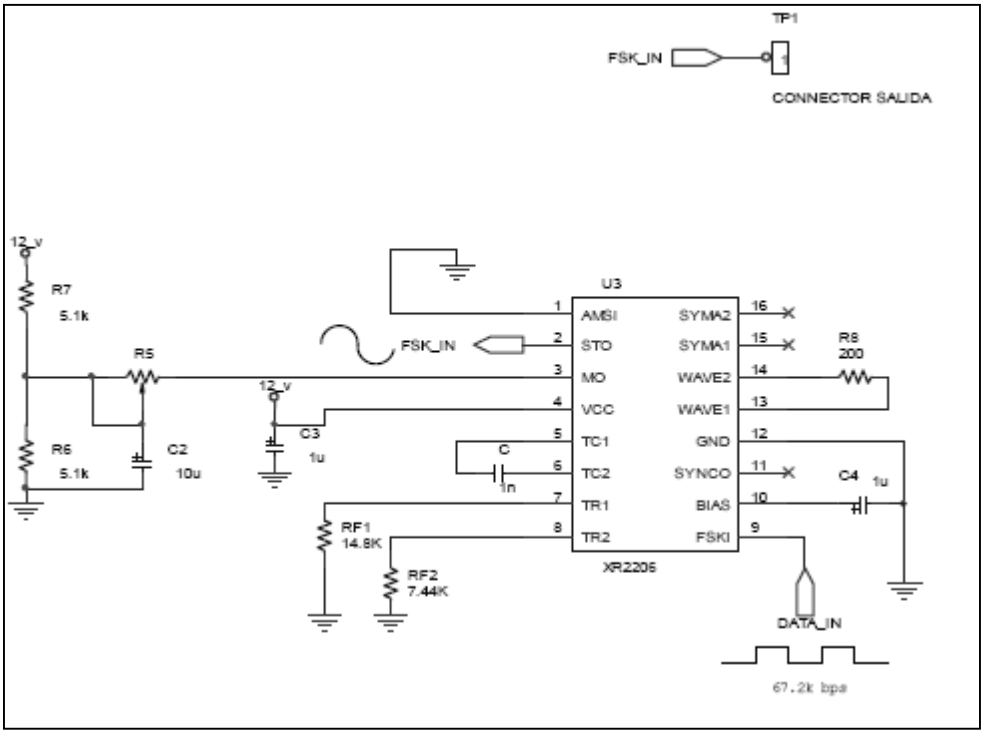
Hay que destacar que las frecuencias en la placa no son las calculadas teóricamente. Esto se debe a que las hemos variado mediante los potenciómetros R1 y R2 para obtener una transmisión y recepción óptima basándonos en la calidad del audio recibido. Los picos laterales se deben también a lo comentado anteriormente: no se trata de una señal sinusoidal perfecta.

1.3. Esquemas

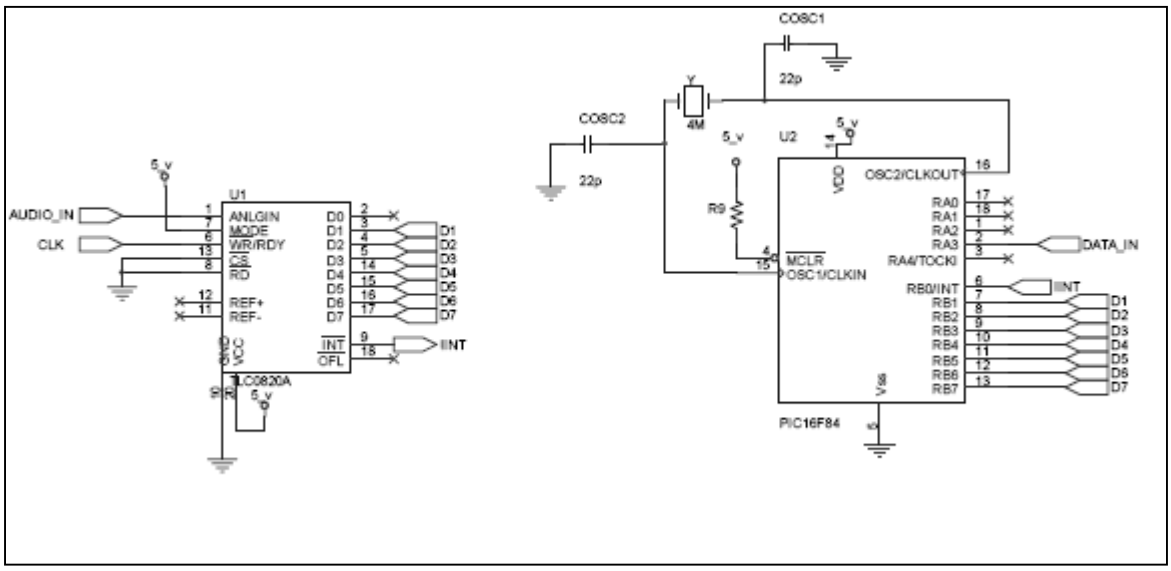
Etapa de Audio y Filtro



Modulador

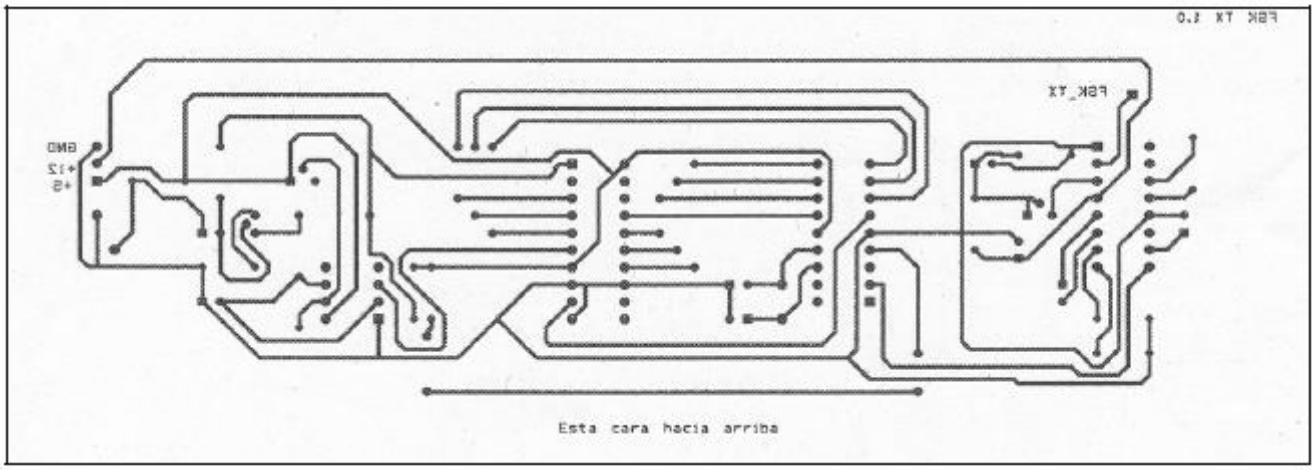


Conversor AD y Microcontrolador PIC

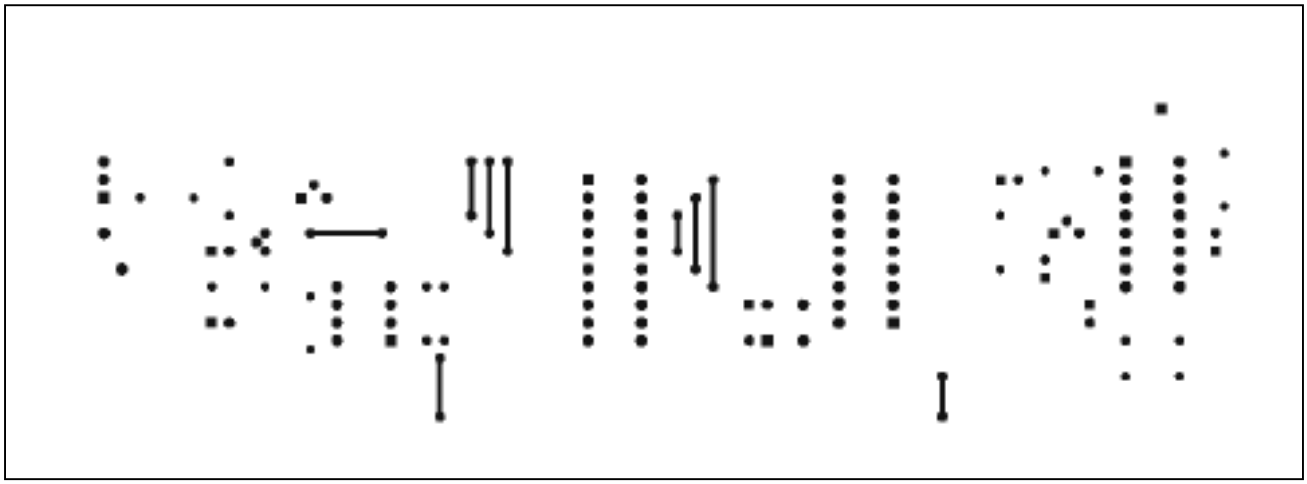


1.4. Layout del Transmisor

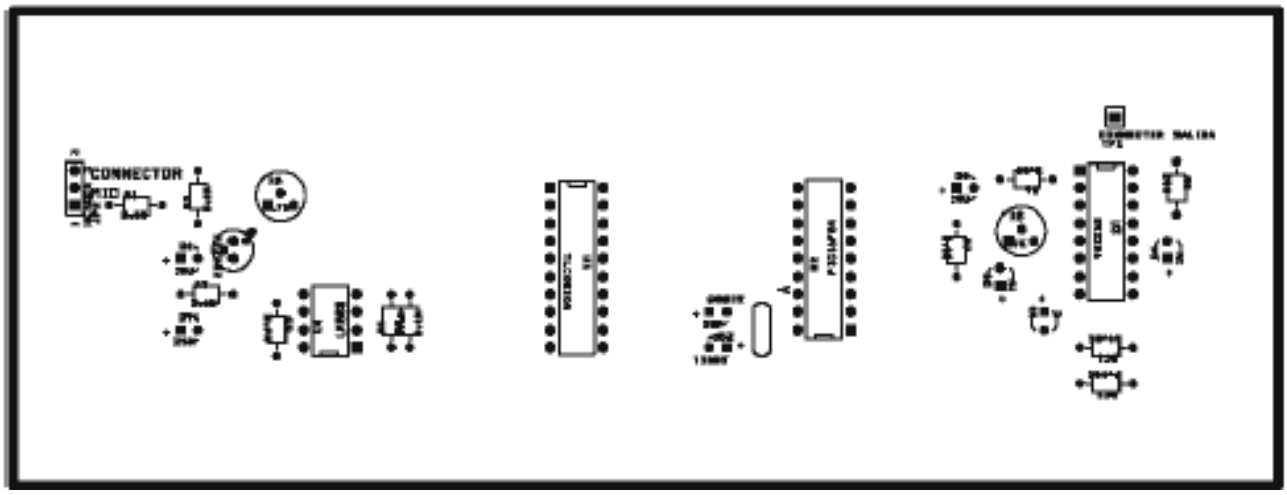
1.4.1. Placa Impresa



1.4.2. Puentes



1.4.3. Posición de los Elementos



1.5. Componentes

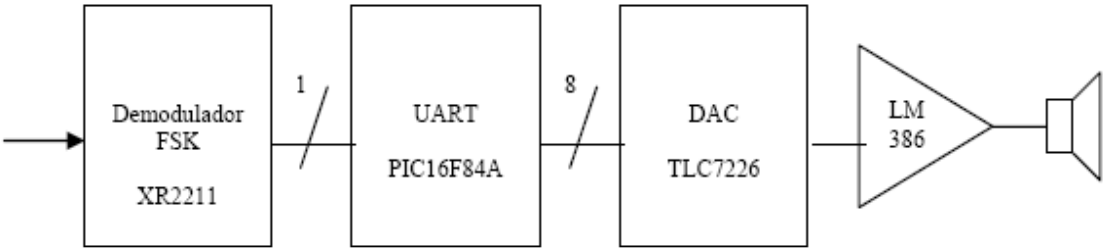
Referencia	Valor
C1	82P
C	1N
C1	10U
C2	10U
C3	1U
C4	1U
CONNECTOR	MIC
COSC1	22P
COSC2	22P
CT1	22N
Q	2N2222
R1	5.1K
R2	5.1K
R3	5.1K
R4	5.1K
R5	50K
R6	5.1K
R7	5.1K
R8	200
R9	5.1K
RA	4.7K
RB	2.7K
RF1	14.8K
RF2	7.44K
U1	TLC0820A
U2	PIC16F84A
U3	XR2206
Y	10M

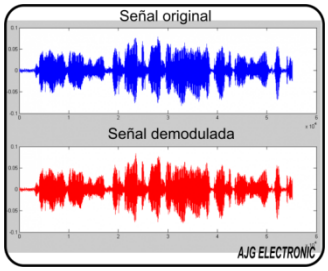
2. Receptor

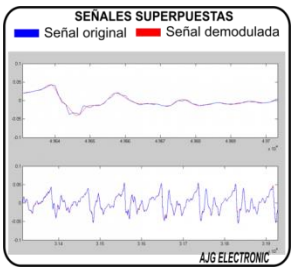
2.1. Funcionamiento

Se trata de un receptor de modulación digital FSK que trabaja a las frecuencias de emisión de 67.2k y 100k.

El esquema del receptor es el siguiente:







2.2. Partes

El diseño está estructurado en cuatro partes bien diferenciadas:

a) El Demodulador.
b) La UART.
c) El convertidor digital – analógico.
d) Amplificador de audio.

2.2.1. El Demodulador

Es la parte más importante del receptor. Se basa en el integrado XR2211 de la casa EXAR. Se trata de un sistema basado en un PLL orientado para comunicaciones en módems.

Como ya se ha comentado, dado que se esta transmitiendo voz sin comprimir se necesita trabajar con frecuencias elevadas en relación con las que habitualmente se usan en modulaciones de este tipo. Este chip dispone de un ancho de banda elevado (0.01kHz – 300kHz) así como de un rango de alimentación adecuado para nuestra aplicación (4.5-20V) que nos permitirá trabajar en TTL.

Para adaptar el integrado a nuestro diseño, el fabricante proporciona una serie de ecuaciones muy útiles. Se detalla a continuación el proceso a seguir:

1. Fijamos el Baud Rate y las frecuencias con las que vamos a trabajar. En nuestro caso:

BR = 67.2kbps
f1 = 67.2kHz
f2 = 100kHz

2. Calculamos la frecuencia central:

$$f_o = \sqrt{f1 \cdot f2} = \mathbf{81.98kHz}$$

3. Calculamos Ro: el fabricante recomienda que el valor de Ro esté entre 10k y 100k. Es un valor que se acabará de fijar en la placa mediante un potenciómetro Rx.

$$Ro = Ro + \frac{Rx}{2} = \mathbf{10K + 5k}$$

4. Calculamos Co:

$$Co = \frac{1}{Ro \cdot fo} = \mathbf{700p}$$

5. Cálculo de R1:

$$R1 = \frac{Ro \cdot fo}{(f1 - f2)} \cdot 2 = \mathbf{74.98K}$$

6. Cálculo C1:

$$C1 = \frac{1250 \cdot Co}{R1 \cdot 0.5^2} = \mathbf{82p}$$

7. Cálculo de RF y RB:

$$R_F = 5 \cdot R1 = \mathbf{212K}$$
$$R_B = 5 \cdot R_F = \mathbf{1.061M}$$

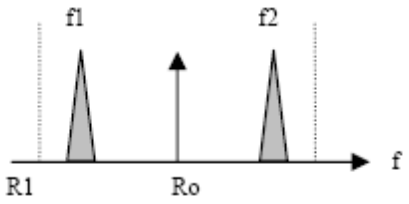
8. Cálculo de RSUM:

$$R_{SUM} = \frac{(R_F + R1) \cdot R_B}{R_F + R1 + R_B} = \mathbf{225.9K}$$

9. Cálculo de Cf:

$$Cf = \frac{0.25}{R_{SUM} \cdot BaudRate} = \mathbf{16.47p}$$

Podemos aproximar todos los valores. En la práctica resulta útil poner potenciómetros para los valores de R1, Ro. Variando R1 estamos fijando el ancho de banda del receptor y con Ro la frecuencia central.

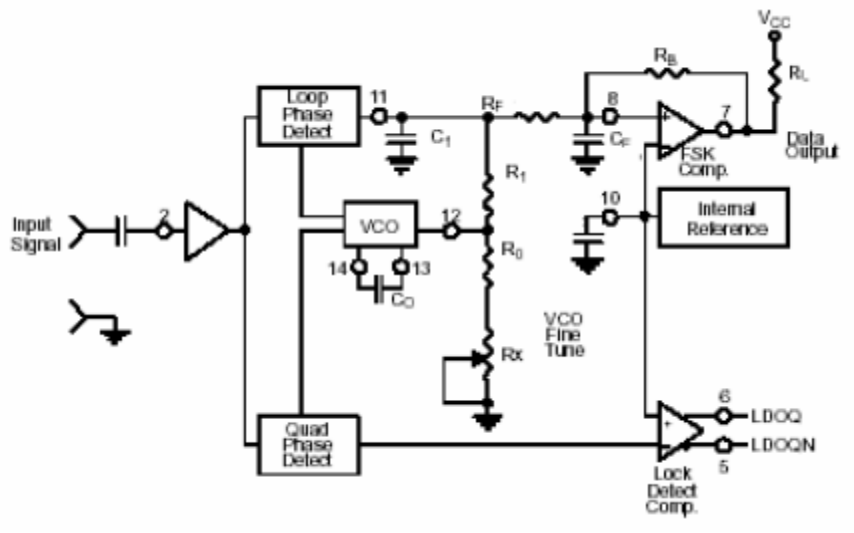


De esta forma controlaremos que tanto emisor y receptor acaben de enganchar el PLL interno del integrado. Esto lo veremos claramente cuando una vez conectados emisor y receptor realicemos la siguiente prueba:

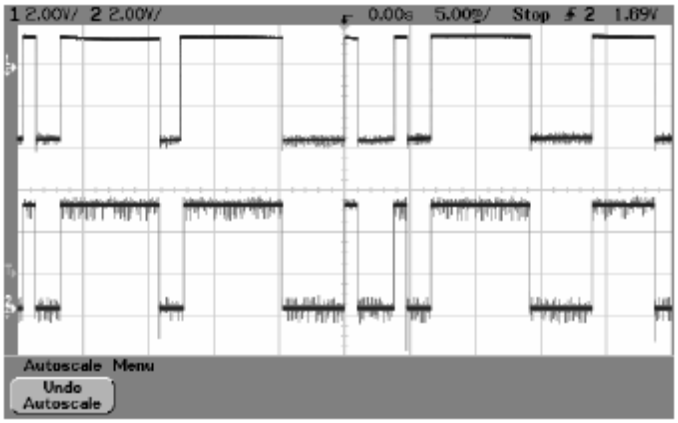
• Poner a la entrada del emisor un “1” constante. El receptor tiene que Demodular un “1” constante.

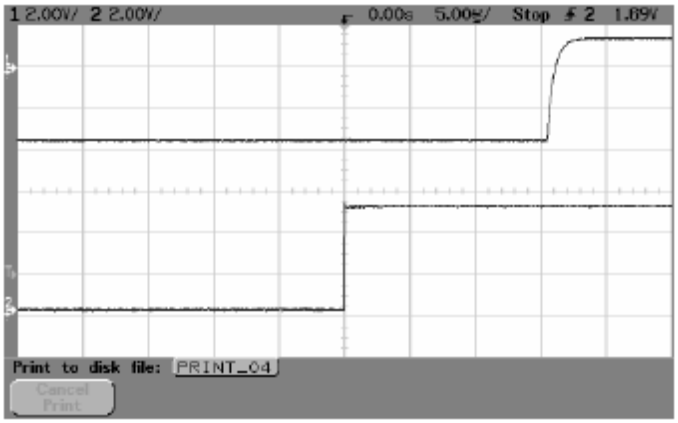
• Poner a la entrada del emisor un “0” constante y recibiendo por el Demodulador un “0” constante también.

Para conseguirlo tendremos que variar los valores de R1 y Ro. Al final veremos como en el pin 13 y 14 (Co) la frecuencia se fija a la del “1” y la del “0” según recibamos uno u otro.



Una vez que la señal ha sido remodulada, medimos el retraso, la introducimos y vemos que es constante para cada bit y de 20µseg. Vemos por tanto que al ser constante y pequeño no nos introducirá grandes problemas en audio.





2.2.2. La UART del Receptor

Como en el caso del emisor la UART ha sido implementada con un microcontrador PIC16F84A. Este integrado nos proporcionado una gran capacidad operativa en un espacio reducido. Su fácil programación hace de él una herramienta indispensable en futuros diseños.

El código es compilable mediante C2C del compilador OPTAMA.

```
#pragma CLOCK_FREQ 10000000
//Configuración para la transmisión serie
#pragma TRUE_RS232 1
#pragma RS232_TXPORT PORTA
#pragma RS232_RXPORT PORTA
#pragma RS232_TXPIN 3
#pragma RS232_RXPIN 2
#pragma RS232_BAUD 67200
//Puerto B de salida
#define PUERTO_A 0x04
#define PUERTO_B 0x00
char data=0;
main () {
disable_interrupt(GIE);
set_bit( STATUS, RP0 );
set_tris_b( PUERTO_B );
set_tris_a( PUERTO_A );
clear_bit( STATUS, RP0 );
for (;;) {
//Con el Puerto A.0 generamos
//la señal !OK
output_high_port_a( 0 );
data=getchar();
output_port_b(data);
output_low_port_a( 0 );
}
}
```

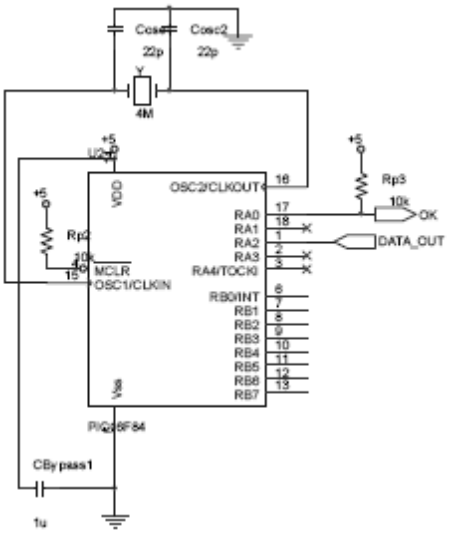
Como se puede ver en el código usaremos el puerto A para recibir los datos en serie con una BR de 67.2k bps. Usaremos también uno de los bits del puerto A para indicar al DAC que puede realizar la conversión porque hemos puesto los datos en el puerto B. Esta señal de control funciona por lógica negativa y es el !WR del DAC.

Es importante destacar que el clock (reloj) trabaja con una frecuencia de 10M cuando el integrado suele funcionar con una de 4M. Esto se debe a la imposibilidad de

realizar los bucles de espera de en la PIC para un bit rate tan elevado. Veamos el código ensamblador de la función delay que implementa el compilador:

```
__c2c_rs232_delay
movlw D'8'
movwf _rs232_delay_counter
label_0005
decfsz _rs232_delay_counter, 1
goto label_0005
return
__c2c_rs232_delay__end
END
```

Vemos que para la función *getchar* se basa en un delay que aplicará a cada bit. Si nuestro clock fuera de 4M, el “8” de la segunda línea se convertiría en un “0”. Por tanto el contador interno de la PIC no crearía un delay proporcional a nuestro Bit rate sino superior ya que daría toda la vuelta completa: de 0 a 255 (0 -> 0xFFh).

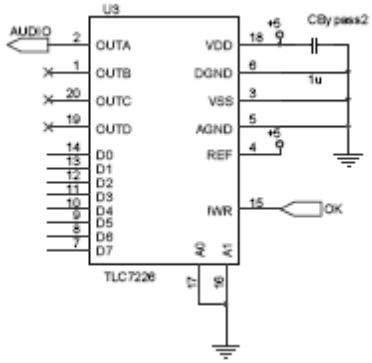


2.2.3. El DAC

Como conversor digital – analógico nos hemos basado en un chip que ya conocíamos (TLC7226 de la casa Texas Instrument) dado que lo usamos en la anterior práctica (osciloscopio digital) y que para su funcionamiento no requiere de elementos externos.

Se trata de un conversor con resolución de 8 bits y de 4 puertos pero que para nuestra aplicación sólo requerimos del primero.

Todas las referencias se han fijado a los valores de tensiones de la placa. Como se ha indicado en el punto anterior, las conversiones se realizarán en basa a la bajada de !WR (PIN-15) que seguirá una frecuencia de unos 8k que es la que origina el emisor para muestrear.



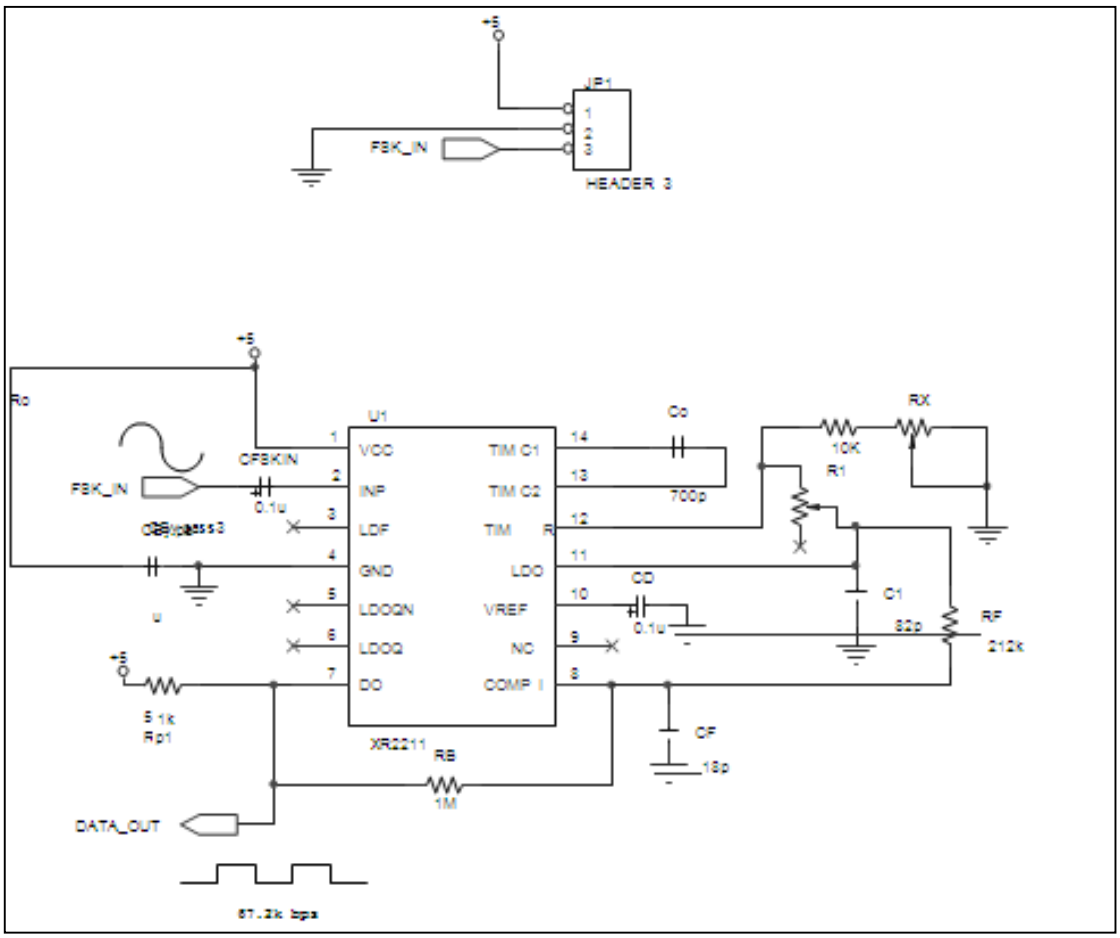
2.2.4. Amplificador de audio

El amplificador de audio es un viejo conocido de las aplicaciones radio que hemos diseñado y que para esta aplicación también le hemos encontrado un espacio. Es un simple integrado de 4 patas con una gran documentación que da fácilmente una ganancia de hasta 20 dB en nuestra configuración.

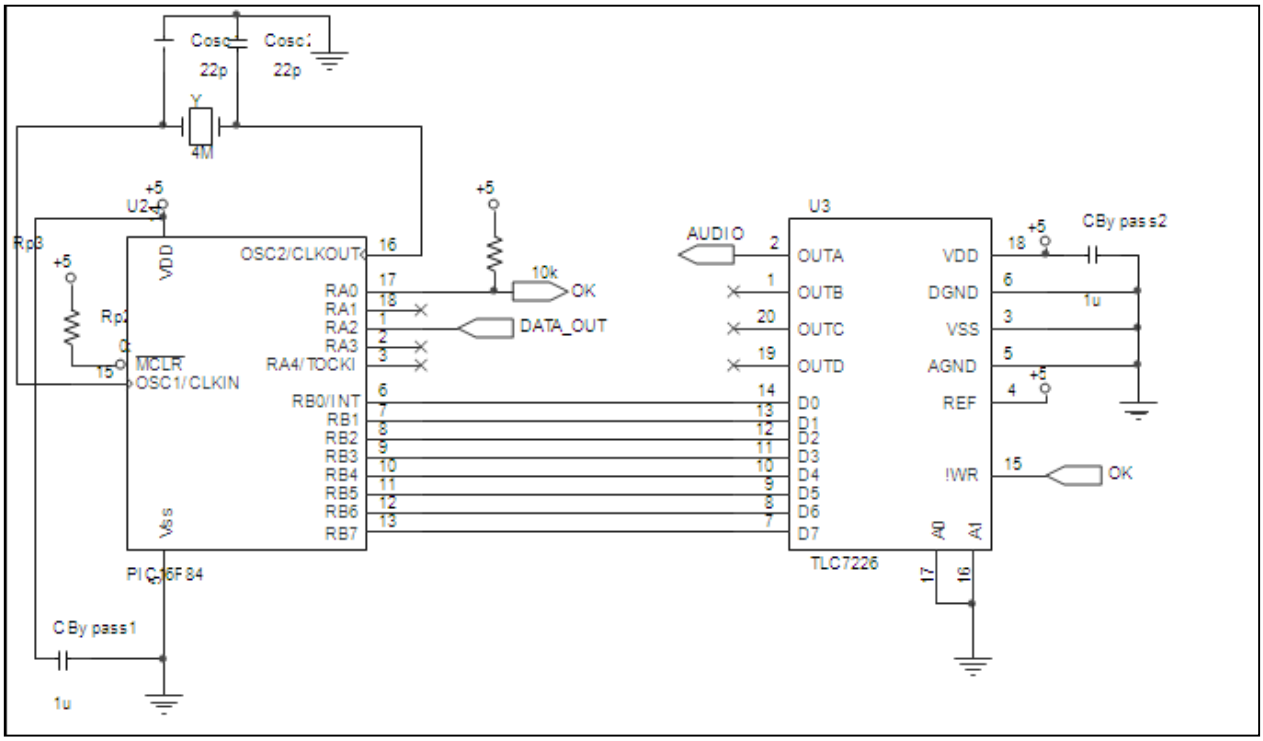
Es útil disponer de un potenciómetro para controlar el volumen y seguir las especificaciones del fabricante para adaptar impedancias con el altavoz y filtrarle la continua, así como proporcionar un filtro de 1º orden a la salida.

2.3. Esquemas

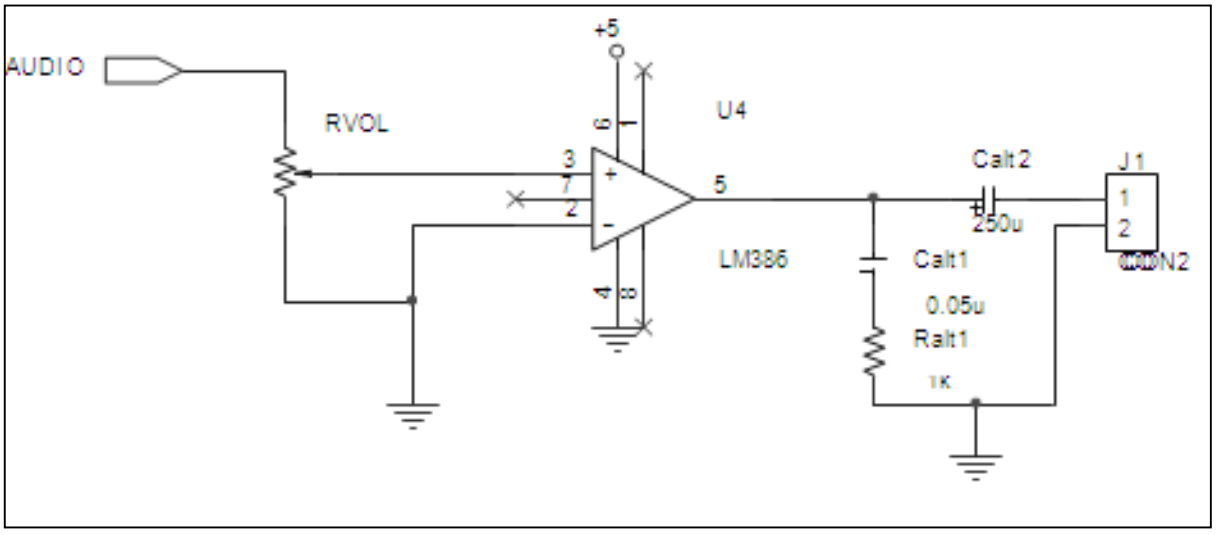
Demodulador



Conversor DA y PIC

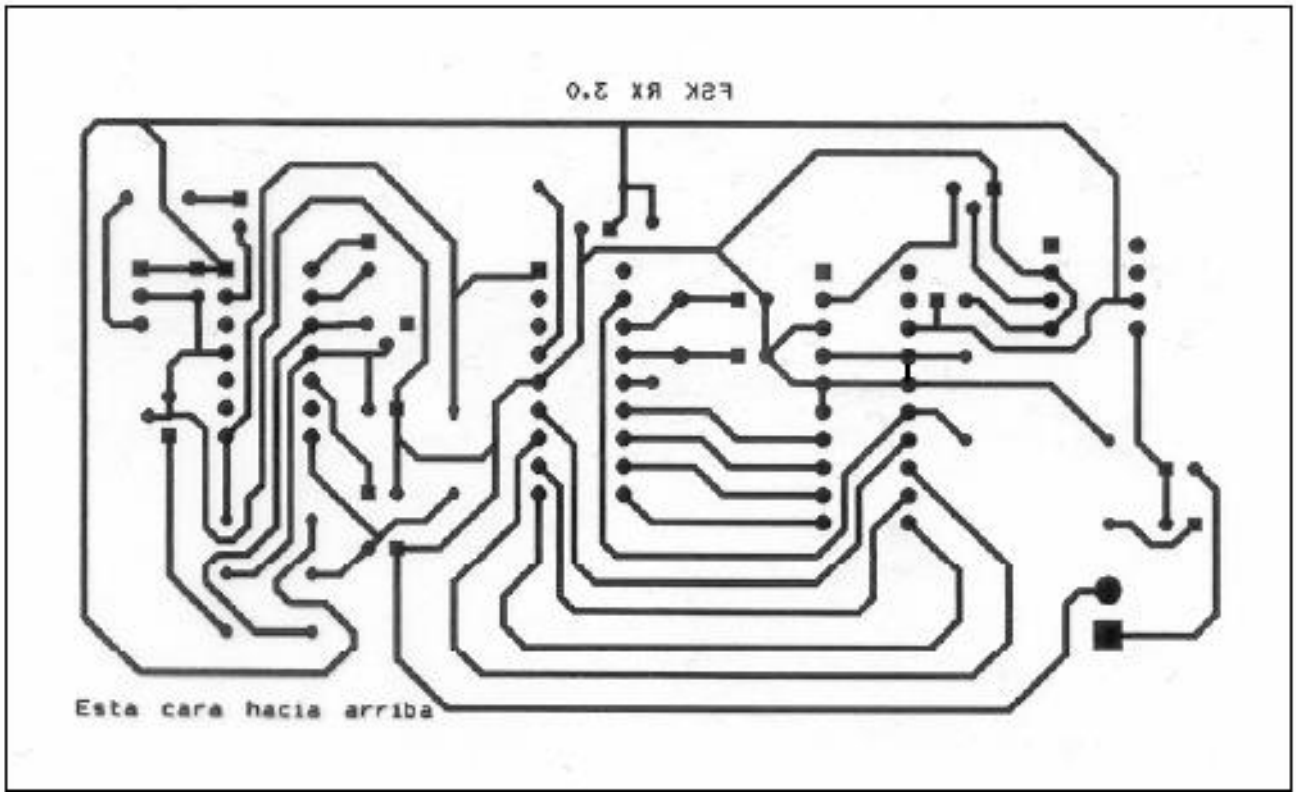


Amplificador de Audio

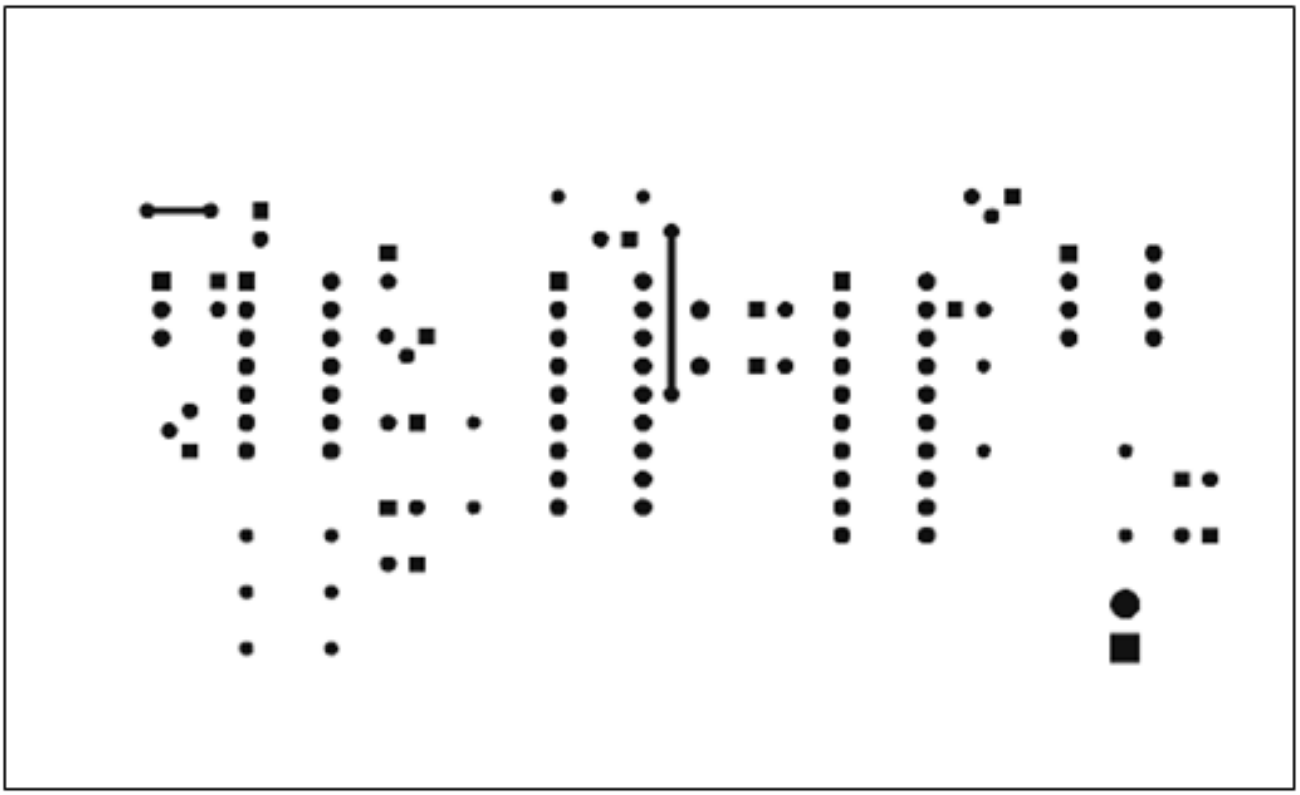


2.4. Layout del Receptor

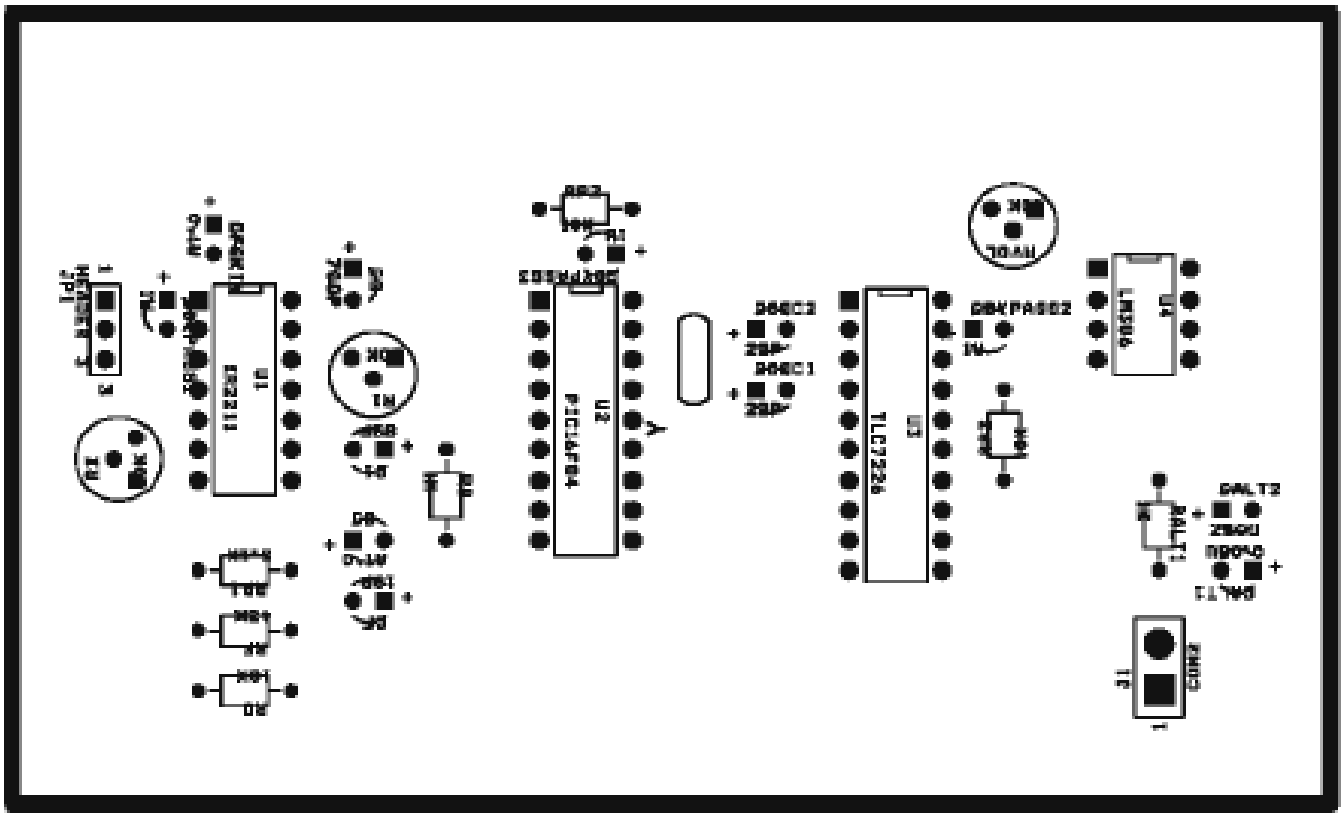
2.4.1. Placa Impresa



2.4. 2. Puentes



2.4.3. Posición de los Elementos



2.5. Componentes

Referencia	Valor
C1	82P
CALT1	0.05U
CALT2	250U
CBYPASS1	1U
CBYPASS2	1U
CBYPASS3	1U
CD	0.1U
CF	18P
CFSKIN	0.1U
CO	700P
COSC1	22P
COSC2	22P
R1	50K
RALT1	1K
RB	1M
RF	43K
RO	10K
RP1	5.1K
RP2	10K
RP3	10K
RVOL	10K
RX	10K
U1	XR2211
U2	PIC16F84
U3	TLC7226
U4	LM386
Y	4M

3. Conclusiones

Los principales problemas con los que nos encontramos a lo largo del desarrollo del proyecto fueron:

• Los condensadores de bypass entre Vcc y Gnd se hacen indispensables en este diseño. La frecuencia de 8k del 555 está presente en toda la alimentación de la placa creando picos de hasta 1V que provoca Reset en el microcontrolador.

• En la etapa de audio es necesario incluir algún tipo de circuito adaptador de impedancias. Concretamente entre el colector del transistor y la entrada del ADC. Este condensador ayuda también a un filtraje antialiasing.

• El modulador y el demodulador se centran en los dos integrados XR. Ha sido necesario acabar de fijar los valores de sus componentes externos mediante potenciómetros. Los valores críticos han sido:

- ✓ R1 y R2 en el modulador para fijar las frecuencias de transmisión.
- ✓ Rx y R1 en el demodulador para fijar la frecuencia central y el ancho de banda.

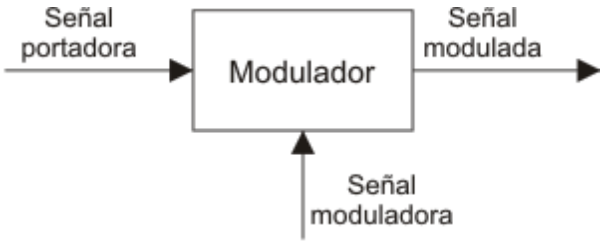
• Se han hecho diversas pruebas de modulación a distintas frecuencias. En un principio se realizaron los cálculos para 67.2k y 138.8k. Debido a que estas frecuencias están muy separadas y a causa de la influencia de la placa de circuito impreso no fue posible enganchar el PLL interno del demodulador. Por tanto se cambiaron los cálculos para frecuencias más próximas.

• Se envió audio sin comprimir a una frecuencia de muestreo de 8k por tanto resultan 64k. Para poder enviar un bit rate de 64k en la PIC fue necesario cambiar el clock de 4M por uno de 10M.

• Se realizaron diversas pruebas del diseño en la tablilla de experimentos (protoboard) y se vio factible aislar el emisor y del receptor. Los cambios producidos en ambas placas han sido recogidos en los últimos esquemas que incluí y se deben principalmente a la falta de condensadores de Bypass.

GLOSARIO

Modulación. Proceso de colocar la información contenida en una señal, generalmente de baja frecuencia, sobre una señal de alta frecuencia. Debido a este proceso la señal de alta frecuencia denominada portadora, sufrirá la modificación de alguna de sus parámetros, siendo dicha modificación proporcional a la amplitud de la señal de baja frecuencia denominada moduladora.



Demodulación. Proceso de recuperación de la señal moduladora de una señal modulada en amplitud (MA) o modulada en frecuencia (MF). El demodulador también es llamado detector.

Frecuencia. Es una magnitud que mide el número de repeticiones por unidad de tiempo de cualquier fenómeno o suceso periódico. La frecuencia se mide en hercios (Hz). Un hercio es aquel suceso o fenómeno repetido una vez por segundo.

Compilar. Proceso de traducción de un código fuente (escrito en un lenguaje de programación de alto nivel) a lenguaje máquina (código objeto) para que pueda ser ejecutado por la computadora. Las computadoras sólo entienden el lenguaje máquina. La aplicación o la herramienta encargada de la traducción se llaman compilador.

Impedancia. La impedancia es la resistencia que opone un componente PASIVO (resistencia, bobina, condensador) al paso de la corriente eléctrica alterna.

DAC. Conversión digital-analógica (del inglés Digital-to-Analog Conversión). Dispositivo que convierte una entrada digital (generalmente binaria) a una señal analógica (generalmente voltaje o carga eléctrica). Los conversores digital-analógico son interfaces entre el mundo abstracto digital y la vida real analógica.

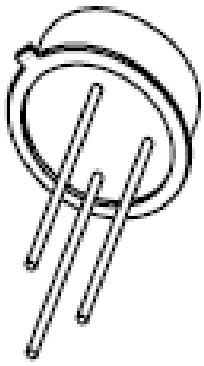
UART. Son las siglas de "Universal Asynchronous Receiver-Transmitter" (en español, Transmisor-Receptor Asíncrono Universal). Éste controla los puertos y dispositivos serie. Se encuentra integrado en la placa base o en la tarjeta adaptadora del dispositivo.

ADC. Conversión analógica - digital (del inglés Analog -to- Digital Conversión). La conversión analógica-digital (CAD) consiste en la transcripción de señales analógicas en señales digitales, con el propósito de facilitar su procesamiento (codificación, compresión, etc.) y hacer la señal resultante (la digital) más inmune al ruido y otras interferencias a las que son más sensibles las señales analógicas.

FSK. El FSK (Frequency-shift keying) es un tipo de modulación de frecuencia cuya señal modulante es un flujo de pulsos binarios que varía entre valores predeterminados. Modulación por desplazamiento de frecuencia o FSK, es una técnica de transmisión digital de información binaria (ceros y unos) utilizando dos frecuencias diferentes. La señal moduladora solo varía entre dos valores de tensión discretos formando un tren de pulsos donde un cero representa un "1" o "marca" y el otro representa el "0" o "espacio".

ANEXOS

DATA SHEET



2N2222; 2N2222A
NPN switching transistors

Product specification
Supersedes data of September 1994
File under Discrete Semiconductors, SC04

1997 May 29

Philips
Semiconductors

PHILIPS

NPN switching transistors 2N2222; 2N2222A

FEATURES

- High current (max. 800 mA)
- Low voltage (max. 40 V).

APPLICATIONS

- Linear amplification and switching.

DESCRIPTION

NPN switching transistor in a TO-18 metal package.
PNP complement: 2N2907A.

PINNING

PIN	DESCRIPTION
1	emitter
2	base
3	collector, connected to case

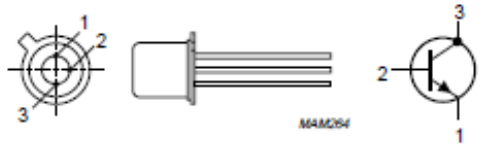


Fig.1 Simplified outline (TO-18) and symbol.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CBO}	collector-base voltage	open emitter			
	2N2222		–	60	V
	2N2222A		–	75	V
V_{CEO}	collector-emitter voltage	open base			
	2N2222		–	30	V
	2N2222A		–	40	V
I_C	collector current (DC)		–	800	mA
P_{tot}	total power dissipation	$T_{amb} \leq 25$ °C	–	500	mW
h_{FE}	DC current gain	I_C = 10 mA; V_{CE} = 10 V	75	–	
f_T	transition frequency	I_C = 20 mA; V_{CE} = 20 V; f = 100 MHz			
	2N2222		250	–	MHz
	2N2222A		300	–	MHz
t_{off}	turn-off time	I_{Con} = 150 mA; I_{Bon} = 15 mA; I_{Boff} = –15 mA	–	250	ns

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CBO}	collector-base voltage	open emitter			
	2N2222		–	60	V
	2N2222A		–	75	V
V_{CEO}	collector-emitter voltage	open base			
	2N2222		–	30	V
	2N2222A		–	40	V
V_{EBO}	emitter-base voltage	open collector			
	2N2222		–	5	V
	2N2222A		–	6	V
I_C	collector current (DC)		–	800	mA
I_{CM}	peak collector current		–	800	mA
I_{BM}	peak base current		–	200	mA
P_{tot}	total power dissipation	$T_{amb} \leq 25$ °C	–	500	mW
		$T_{case} \leq 25$ °C	–	1.2	W
T_{stg}	storage temperature		–65	+150	°C
T_j	junction temperature		–	200	°C
T_{amb}	operating ambient temperature		–65	+150	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient	in free air	350	K/W
$R_{th\ j\text{-}c}$	thermal resistance from junction to case		146	K/W

CHARACTERISTICS

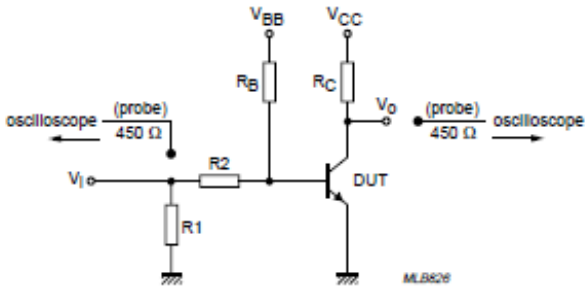
T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
I_{CBO}	collector cut-off current				
	2N2222	I_E = 0; V_{CB} = 50 V	–	10	nA
		I_E = 0; V_{CB} = 50 V; T_{amb} = 150 °C	–	10	µA
I_{CBO}	collector cut-off current				
	2N2222A	I_E = 0; V_{CB} = 60 V	–	10	nA
		I_E = 0; V_{CB} = 60 V; T_{amb} = 150 °C	–	10	µA
I_{EBO}	emitter cut-off current	I_C = 0; V_{EB} = 3 V	–	10	nA
h_{FE}	DC current gain	I_C = 0.1 mA; V_{CE} = 10 V	35	–	
		I_C = 1 mA; V_{CE} = 10 V	50	–	
		I_C = 10 mA; V_{CE} = 10 V	75	–	
		I_C = 150 mA; V_{CE} = 1 V; note 1	50	–	
		I_C = 150 mA; V_{CE} = 10 V; note 1	100	300	
h_{FE}	DC current gain	I_C = 10 mA; V_{CE} = 10 V; T_{amb} = –55 °C			
	2N2222A		35	–	
h_{FE}	DC current gain	I_C = 500 mA; V_{CE} = 10 V; note 1			
	2N2222		30	–	
	2N2222A		40	–	
V_{CEsat}	collector-emitter saturation voltage				
	2N2222	I_C = 150 mA; I_B = 15 mA; note 1	–	400	mV
		I_C = 500 mA; I_B = 50 mA; note 1	–	1.6	V
V_{CEsat}	collector-emitter saturation voltage				
	2N2222A	I_C = 150 mA; I_B = 15 mA; note 1	–	300	mV
		I_C = 500 mA; I_B = 50 mA; note 1	–	1	V
V_{BEsat}	base-emitter saturation voltage				
	2N2222	I_C = 150 mA; I_B = 15 mA; note 1	–	1.3	V
		I_C = 500 mA; I_B = 50 mA; note 1	–	2.6	V
V_{BEsat}	base-emitter saturation voltage				
	2N2222A	I_C = 150 mA; I_B = 15 mA; note 1	0.6	1.2	V
		I_C = 500 mA; I_B = 50 mA; note 1	–	2	V
C_c	collector capacitance	I_E = i_e = 0; V_{CB} = 10 V; f = 1 MHz	–	8	pF
C_e	emitter capacitance	I_C = i_c = 0; V_{EB} = 500 mV; f = 1 MHz			
	2N2222A		–	25	pF
f_T	transition frequency	I_C = 20 mA; V_{CE} = 20 V; f = 100 MHz			
	2N2222		250	–	MHz
	2N2222A		300	–	MHz
F	noise figure	I_C = 200 µA; V_{CE} = 5 V; R_S = 2 kΩ;			
	2N2222A	f = 1 kHz; B = 200 Hz	–	4	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
Switching times (between 10% and 90% levels); see Fig.2					
t_{on}	turn-on time	I_{Con} = 150 mA; I_{Bon} = 15 mA; I_{Boff} = −15 mA	–	35	ns
t_d	delay time		–	10	ns
t_r	rise time		–	25	ns
t_{off}	turn-off time		–	250	ns
t_s	storage time		–	200	ns
t_f	fall time		–	60	ns

Note

1. Pulse test: $t_p \leq 300\ \mu s$; $\delta \leq 0.02$.



V_I = 9.5 V; T = 500 µs; t_p = 10 µs; t_r = $t_f \leq$ 3 ns.
R1 = 68 Ω; R2 = 325 Ω; R_B = 325 Ω; R_C = 160 Ω.
V_{BB} = −3.5 V; V_{CC} = 29.5 V.
Oscilloscope input impedance Z_i = 50 Ω.

Fig.2 Test circuit for switching times.

AMPLIFICADOR LM386

National Semiconductor

January 2000

LM386
Low Voltage Audio Power Amplifier

General Description

The LM386 is a power amplifier designed for use in low voltage consumer applications. The gain is internally set to 20 to keep external part count low, but the addition of an external resistor and capacitor between pins 1 and 8 will increase the gain to any value up to 200.

The inputs are ground referenced while the output is automatically biased to one half the supply voltage. The quiescent power drain is only 24 milliwatts when operating from a 6 volt supply, making the LM386 ideal for battery operation.

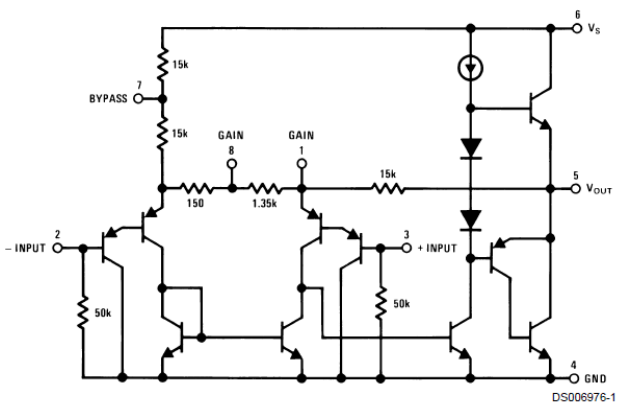
Features

- Battery operation
- Minimum external parts
- Wide supply voltage range: 4V–12V or 5V–18V
- Low quiescent current drain: 4 mA
- Voltage gains from 20 to 200
- Ground referenced input
- Self-centering output quiescent voltage
- Low distortion
- Available in 8 pin MSOP package

Applications

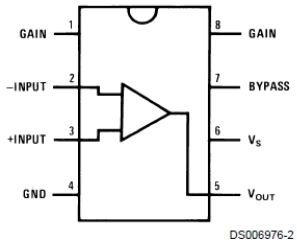
- AM-FM radio amplifiers
- Portable tape player amplifiers
- Intercoms
- TV sound systems
- Line drivers
- Ultrasonic drivers
- Small servo drivers
- Power converters

Equivalent Schematic and Connection Diagrams



DS006976-1

Small Outline, Molded Mini Small Outline, and Dual-In-Line Packages



DS006976-2

Top View
Order Number LM386M-1, LM386MM-1, LM386N-1, LM386N-3 or LM386N-4
See NS Package Number M08A, MUA08A or N08E

Absolute Maximum Ratings (Note 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	
(LM386N-1, -3, LM386M-1)	15V
Supply Voltage (LM386N-4)	22V
Package Dissipation (Note 3)	
(LM386N)	1.25W
(LM386M)	0.73W
(LM386MM-1)	0.595W
Input Voltage	±0.4V
Storage Temperature	−65°C to +150°C
Operating Temperature	0°C to +70°C
Junction Temperature	+150°C
Soldering Information	
Dual-In-Line Package	
Soldering (10 sec)	+260°C
Small Outline Package	
(SOIC and MSOP)	
Vapor Phase (60 sec)	+215°C
Infrared (15 sec)	+220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

Thermal Resistance	
θ_{JC} (DIP)	37°C/W
θ_{JA} (DIP)	107°C/W
θ_{JC} (SO Package)	35°C/W
θ_{JA} (SO Package)	172°C/W
θ_{JA} (MSOP)	210°C/W
θ_{JC} (MSOP)	56°C/W

Electrical Characteristics (Notes 1, 2)

T_A = 25°C

Parameter	Conditions	Min	Typ	Max	Units
Operating Supply Voltage (V_S)					
LM386N-1, -3, LM386M-1, LM386MM-1		4		12	V
LM386N-4		5		18	V
Quiescent Current (I_Q)	V_S = 6V, V_{IN} = 0		4	8	mA
Output Power (P_{OUT})					
LM386N-1, LM386M-1, LM386MM-1	V_S = 6V, R_L = 8Ω, THD = 10%	250	325		mW
LM386N-3	V_S = 9V, R_L = 8Ω, THD = 10%	500	700		mW
LM386N-4	V_S = 16V, R_L = 32Ω, THD = 10%	700	1000		mW
Voltage Gain (A_V)	V_S = 6V, f = 1 kHz		26		dB
	10 µF from Pin 1 to 8		46		dB
Bandwidth (BW)	V_S = 6V, Pins 1 and 8 Open		300		kHz
Total Harmonic Distortion (THD)	V_S = 6V, R_L = 8Ω, P_{OUT} = 125 mW		0.2		%
	f = 1 kHz, Pins 1 and 8 Open				
Power Supply Rejection Ratio (PSRR)	V_S = 6V, f = 1 kHz, C_{BYPASS} = 10 µF		50		dB
	Pins 1 and 8 Open, Referred to Output				
Input Resistance (R_{IN})			50		kΩ
Input Bias Current (I_{BIAS})	V_S = 6V, Pins 2 and 3 Open		250		nA

Note 1: All voltages are measured with respect to the ground pin, unless otherwise specified.

Note 2: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. Electrical Characteristics state DC and AC electrical specifications under particular test conditions which guarantee specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not guaranteed for parameters where no limit is given, however, the typical value is a good indication of device performance.

Note 3: For operation in ambient temperatures above 25°C, the device must be derated based on a 150°C maximum junction temperature and 1) a thermal resistance of 107°C/W junction to ambient for the dual-in-line package and 2) a thermal resistance of 170°C/W for the small outline package.

Application Hints

GAIN CONTROL

To make the LM386 a more versatile amplifier, two pins (1 and 8) are provided for gain control. With pins 1 and 8 open the 1.35 kΩ resistor sets the gain at 20 (26 dB). If a capacitor is put from pin 1 to 8, bypassing the 1.35 kΩ resistor, the gain will go up to 200 (46 dB). If a resistor is placed in series with the capacitor, the gain can be set to any value from 20 to 200. Gain control can also be done by capacitively coupling a resistor (or FET) from pin 1 to ground.

Additional external components can be placed in parallel with the internal feedback resistors to tailor the gain and frequency response for individual applications. For example, we can compensate poor speaker bass response by frequency shaping the feedback path. This is done with a series RC from pin 1 to 5 (paralleling the internal 15 kΩ resistor). For 6 dB effective bass boost: R ≅ 15 kΩ, the lowest value for good stable operation is R = 10 kΩ if pin 8 is open. If pins 1 and 8 are bypassed then R as low as 2 kΩ can be used. This restriction is because the amplifier is only compensated for closed-loop gains greater than 9.

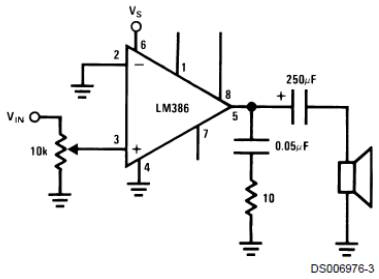
INPUT BIASING

The schematic shows that both inputs are biased to ground with a 50 kΩ resistor. The base current of the input transistors is about 250 nA, so the inputs are at about 12.5 mV when left open. If the dc source resistance driving the LM386 is higher than 250 kΩ it will contribute very little additional offset (about 2.5 mV at the input, 50 mV at the output). If the dc source resistance is less than 10 kΩ, then shorting the unused input to ground will keep the offset low (about 2.5 mV at the input, 50 mV at the output). For dc source resistances between these values we can eliminate excess offset by putting a resistor from the unused input to ground, equal in value to the dc source resistance. Of course all offset problems are eliminated if the input is capacitively coupled.

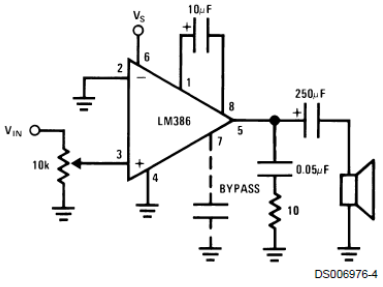
When using the LM386 with higher gains (bypassing the 1.35 kΩ resistor between pins 1 and 8) it is necessary to bypass the unused input, preventing degradation of gain and possible instabilities. This is done with a 0.1 µF capacitor or a short to ground depending on the dc source resistance on the driven input.

Typical Applications

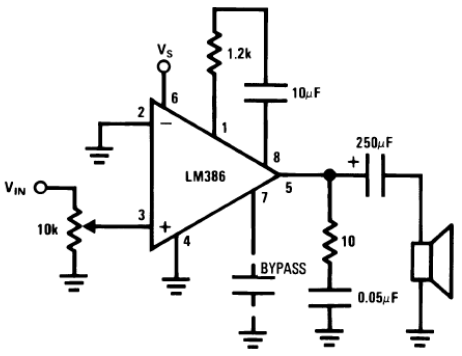
Amplifier with Gain = 20
Minimum Parts



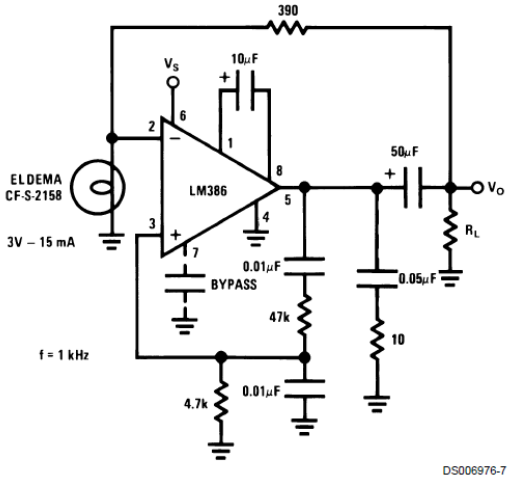
Amplifier with Gain = 200



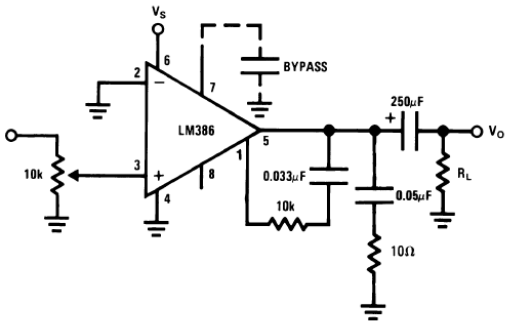
Amplifier with Gain = 50



Low Distortion Power Wienbridge Oscillator

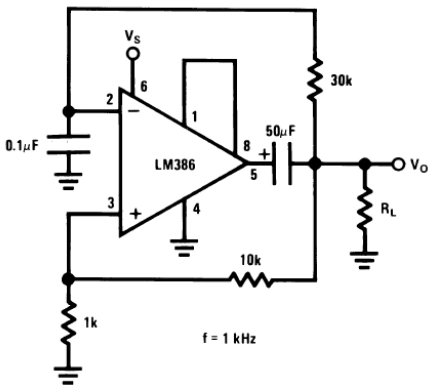


Amplifier with Bass Boost



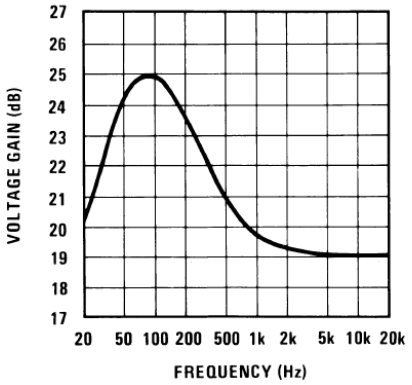
DS006976-8

Square Wave Oscillator



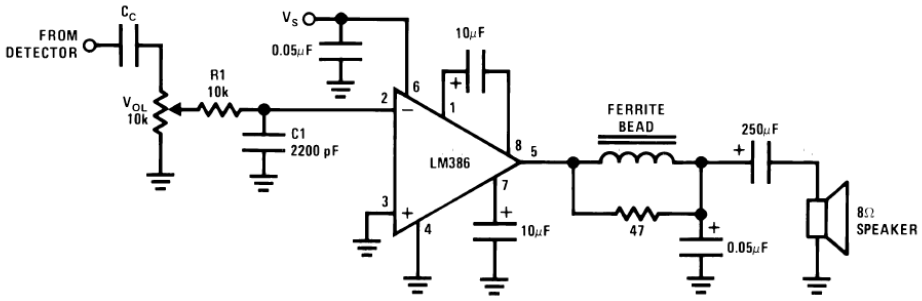
DS006976-9

Frequency Response with Bass Boost



DS006976-10

AM Radio Power Amplifier



DS006976-11

Note 4: Twist Supply lead and supply ground very tightly.

Note 5: Twist speaker lead and ground very tightly.

Note 6: Ferrite bead in Ferroxcube K5-001-001/3B with 3 turns of wire.

Note 7: R1C1 band limits input signals.

Note 8: All components must be spaced very closely to IC.

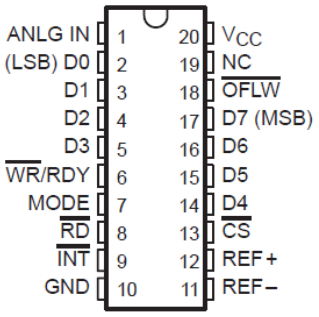
CONVERSOR A/D TLC0820AC

TLC0820AC, TLC0820AI
Advanced LinCMOS™ HIGH-SPEED 8-BIT ANALOG-TO-DIGITAL CONVERTERS USING MODIFIED FLASH TECHNIQUES

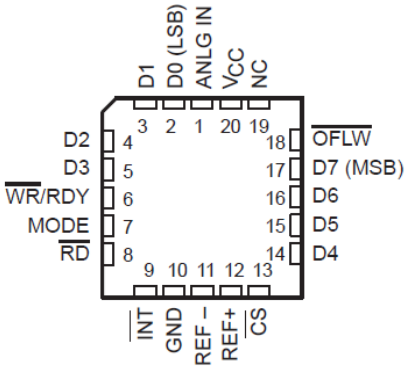
SLAS064A – SEPTEMBER 1986 – REVISED JUNE 1994

- Advanced LinCMOS™ Silicon-Gate Technology
- 8-Bit Resolution
- Differential Reference Inputs
- Parallel Microprocessor Interface
- Conversion and Access Time Over Temperature Range
  Read Mode . . . 2.5 µs Max
- No External Clock or Oscillator Components Required
- On-Chip Track and Hold
- Single 5-V Supply
- TLC0820A Is Direct Replacement for National Semiconductor ADC0820C/CC and Analog Devices AD7820K/B/T

DB, DW, OR N PACKAGE
(TOP VIEW)



FN PACKAGE
(TOP VIEW)



NC – No internal connection

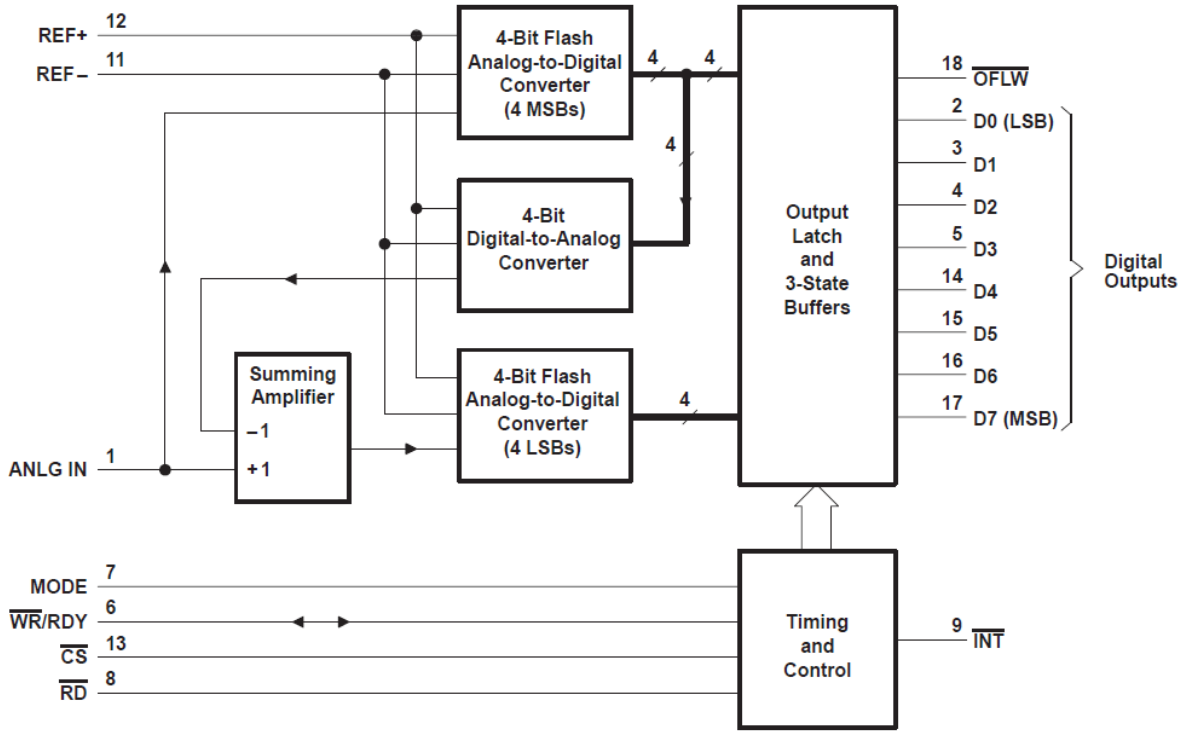
description

The TLC0820AC and the TLC0820AI are Advanced LinCMOS™ 8-bit analog-to-digital converters each consisting of two 4-bit flash converters, a 4-bit digital-to-analog converter, a summing (error) amplifier, control logic, and a result latch circuit. The modified flash technique allows low-power integrated circuitry to complete an 8-bit conversion in 1.18 µs over temperature. The on-chip track-and-hold circuit has a 100-ns sample window and allows these devices to convert continuous analog signals having slew rates of up to 100 mV/µs without external sampling components. TTL-compatible 3-state output drivers and two modes of operation allow interfacing to a variety of microprocessors. Detailed information on interfacing to most popular microprocessors is readily available from the factory.

AVAILABLE OPTIONS

T_A	TOTAL UNADJUSTED ERROR	PACKAGE			
		SSOP (DB)	PLASTIC SMALL OUTLINE (DW)	PLASTIC CHIP CARRIER (FN)	PLASTIC DIP (N)
0°C to 70°C	±1 LSB	TLC0820ACDB	TLC0820ACDW	TLC0820ACFN	TLC0820ACN
–40°C to 85°C	±1 LSB	—	TLC0820AIDW	TLC0820AIFN	TLC0820AIN

functional block diagram



Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
ANLG IN	1	I	Analog input
$\overline{CS}$	13	I	Chip select. $\overline{CS}$ must be low in order for $\overline{RD}$ or $\overline{WR}$ to be recognized by the ADC.
D0	2	O	Digital, 3-state output data, bit 1 (LSB)
D1	3	O	Digital, 3-state output data, bit 2
D2	4	O	Digital, 3-state output data, bit 3
D3	5	O	Digital, 3-state output data, bit 4
D4	14	O	Digital, 3-state output data, bit 5
D5	15	O	Digital, 3-state output data, bit 6
D6	16	O	Digital, 3-state output data, bit 7
D7	17	O	Digital, 3-state output data, bit 8 (MSB)
GND	10		Ground
$\overline{INT}$	9	O	Interrupt. In the write-read mode, the interrupt output ($\overline{INT}$) going low indicates that the internal count-down delay time, $t_{d(int)}$, is complete and the data result is in the output latch. The delay time $t_{d(int)}$ is typically 800 ns starting after the rising edge of $\overline{WR}$ (see operating characteristics and Figure 3). If $\overline{RD}$ goes low prior to the end of $t_{d(int)}$, $\overline{INT}$ goes low at the end of $t_{d(RI)}$ and the conversion results are available sooner (see Figure 2). $\overline{INT}$ is reset by the rising edge of either $\overline{RD}$ or $\overline{CS}$.
MODE	7	I	Mode select. MODE is internally tied to GND through a 50-μA current source, which acts like a pulldown resistor. When MODE is low, the read mode is selected. When MODE is high, the write-read mode is selected.
NC	19		No internal connection
$\overline{OFLW}$	18	O	Overflow. Normally $\overline{OFLW}$ is a logical high. However, if the analog input is higher than V_{ref+}, $\overline{OFLW}$ will be low at the end of conversion. It can be used to cascade two or more devices to improve resolution (9 or 10 bits).
$\overline{RD}$	8	I	Read. In the write-read mode with $\overline{CS}$ low, the 3-state data outputs D0 through D7 are activated when $\overline{RD}$ goes low. $\overline{RD}$ can also be used to increase the conversion speed by reading data prior to the end of the internal count-down delay time. As a result, the data transferred to the output latch is latched after the falling edge of $\overline{RD}$. In the read mode with $\overline{CS}$ low, the conversion starts with $\overline{RD}$ going low. $\overline{RD}$ also enables the 3-state data outputs on completion of the conversion. RDY going into the high-impedance state and $\overline{INT}$ going low indicate completion of the conversion.
REF−	11	I	Reference voltage. REF− is placed on the bottom of the resistor ladder.
REF+	12	I	Reference voltage. REF+ is placed on the top of the resistor ladder.
V_{CC}	20		Power supply voltage
$\overline{WR}$/RDY	6	I/O	Write ready. In the write-read mode with $\overline{CS}$ low, the conversion is started on the falling edge of the $\overline{WR}$ input signal. The result of the conversion is strobed into the output latch after the internal count-down delay time, $t_{d(int)}$, provided that the $\overline{RD}$ input does not go low prior to this time. The delay time $t_{d(int)}$ is approximately 800 ns. In the read mode, RDY (an open-drain output) goes low after the falling edge of $\overline{CS}$ and goes into the high-impedance state when the conversion is strobed into the output latch. It is used to simplify the interface to a microprocessor system.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1) . . . . . 10 V
Input voltage range, all inputs (see Note 1) . . . . . −0.2 V to V_{CC}+0.2 V
Output voltage range, all outputs (see Note 1) . . . . . −0.2 V to V_{CC}+0.2 V
Operating free-air temperature range: TLC0820AC . . . . . 0°C to 70°C
TLC0820AI . . . . . −40°C to 85°C
Storage temperature range . . . . . −65°C to 150°C
Case temperature for 10 seconds: FN package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: DB, DW or N package . . . . . 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltages are with respect to network GND.

recommended operating conditions

			MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}			4.5	5	8	V
Analog input voltage			−0.1		V_{CC}+0.1	V
Positive reference voltage, V_{ref+}			V_{ref-}		V_{CC}	V
Negative reference voltage, V_{ref-}			GND		V_{ref+}	V
High-level input voltage, V_{IH}	V_{CC} = 4.75 V to 5.25 V	$\overline{CS}$, $\overline{WR}$/RDY, $\overline{RD}$	2			V
		MODE	3.5			
Low-level input voltage, V_{IL}	V_{CC} = 4.75 V to 5.25 V	$\overline{CS}$, $\overline{WR}$/RDY, $\overline{RD}$			0.8	V
		MODE			1.5	
Pulse duration, write in write-read mode, $t_{w(W)}$ (see Figures 2, 3, and 4)			0.5		50	µs
Operating free-air temperature, T_A	TLC0820AC		0		70	°C
	TLC0820AI		−40		85	

electrical characteristics at specified operating free-air temperature, V_{CC} = 5 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	T_A†	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	D0–D7, $\overline{INT}$, or $\overline{OFLW}$	V_{CC} = 4.75 V, I_{OH} = −360 µA	Full range	2.4			V
			V_{CC} = 4.75 V, I_{OH} = −10 µA	Full range	4.5			
				25°C	4.6			
V_{OL}	Low-level output voltage	D0–D7, $\overline{OFLW}$, $\overline{INT}$, or $\overline{WR}$/RDY	V_{CC} = 5.25 V, I_{OL} = 1.6 mA	Full range			0.4	V
				25°C			0.34	
I_{IH}	High-level input current	$\overline{CS}$ or $\overline{RD}$	V_{IH} = 5 V	Full range		0.005	1	µA
		WR/RDY		Full range			3	
				25°C		0.1	0.3	
		MODE		Full range			200	
				25°C		50	170	
I_{IL}	Low-level input current	$\overline{CS}$, $\overline{WR}$/RDY, $\overline{RD}$, or MODE	V_{IL} = 0	Full range		−0.005	−1	µA
I_{OZ}	Off-state (high-impedance-state) output current	D0–D7 or $\overline{WR}$/RDY	V_O = 5 V	Full range			3	µA
				25°C		0.1	0.3	
			V_O = 0	Full range			−3	
				25°C		−0.1	−0.3	
I_I	Analog input current		CS at 5 V, V_I = 5 V	Full range			3	µA
				25°C			0.3	
			CS at 5 V, V_I = 0	Full range			−3	
				25°C			−0.3	
I_{OS}	Short-circuit output current	D0–D7, $\overline{OFLW}$, $\overline{INT}$, or $\overline{WR}$/RDY	V_O = 5 V	Full range	7			mA
				25°C	8.4	14		
		D0–D7 or $\overline{OFLW}$	V_O = 0	Full range	−6			
				25°C	−7.2	−12		
		INT		Full range	−4.5			
				25°C	−5.3	−9		
R_{ref}	Reference resistance			Full range	1.25		6	kΩ
				25°C	1.4	2.3	5.3	
I_{CC}	Supply current		$\overline{CS}$, $\overline{WR}$/RDY, and $\overline{RD}$ at 0 V	Full range			15	mA
				25°C		7.5	13	
C_i	Input capacitance	D0–D7		Full range		5		pF
		ANLG IN				45		
C_o	Output capacitance	D0–D7		Full range			5	pF

† Full range is as specified in recommended operating conditions.

operating characteristics, V_{CC} = 5 V, V_{ref+} = 5 V, V_{ref-} = 0, $t_r = t_f$ = 20 ns, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MIN	TYP	MAX	UNIT
k_{SVS}	Supply-voltage sensitivity	V_{CC} = 5 V ± 5%,	T_A = MIN to MAX		±1/16	±1/4	LSB
	Total unadjusted error‡	MODE at 0 V,	T_A = MIN to MAX			1	LSB
$t_{conv(R)}$	Conversion time, read mode	MODE at 0 V,	See Figure 1		1.6	2.5	µs
$t_{a(R)}$	Access time, $\overline{RD}$↓ to data valid	MODE at 0 V,	See Figure 1		$t_{conv(R)}$ +20	$t_{conv(R)}$ +50	ns
$t_{a(R1)}$	Access time, $\overline{RD}$↓ to data valid	MODE at 5 V, $t_{d(WR)} < t_{d(int)}$, See Figure 2	C_L = 15 pF		190	280	ns
			C_L = 100 pF		210	320	
$t_{a(R2)}$	Access time, $\overline{RD}$↓ to data valid	MODE at 5 V, $t_{d(WR)} > t_{d(int)}$, See Figure 3	C_L = 15 pF		70	120	ns
			C_L = 100 pF		90	150	
$t_{a(INT)}$	Access time, $\overline{INT}$↓ to data valid	MODE at 5 V,	See Figure 4		20	50	ns
t_{dis}	Disable time, $\overline{RD}$↑ to data valid	R_L = 1 kΩ, See Figures 1, 2, 3, and 5	C_L = 10 pF,		70	95	ns
$t_{d(int)}$	Delay time, WR/RDY↑ to INT↓	MODE at 5 V, See Figures 2, 3, and 4	C_L = 50 pF,		800	1300	ns
$t_{d(NC)}$	Delay time, to next conversion	See Figures 1, 2, 3, and 4		500			ns
$t_{d(WR)}$	Delay time, $\overline{WR}$/RDY↑ to $\overline{RD}$↓ in write-read mode	See Figure 2		0.4			µs
$t_{d(RDY)}$	Delay time, CS↓ to WR/RDY↓	MODE at 0 V, See Figure 1	C_L = 50 pF,		50	100	ns
$t_{d(RIH)}$	Delay time, $\overline{RD}$↑ to $\overline{INT}$↑	C_L = 50 pF,	See Figures 1, 2, and 3		125	225	ns
$t_{d(RIL)}$	Delay time, RD↓ to INT↓	MODE at 5 V, See Figure 2	$t_{d(WR)} < t_{d(int)}$,		200	290	ns
$t_{d(WIH)}$	Delay time, $\overline{WR}$/RDY↑ to $\overline{INT}$↑	MODE at 5 V, See Figure 4	C_L = 50 pF,		175	270	ns
	Slew-rate tracking				0.1		V/µs

APPLICATION INFORMATION

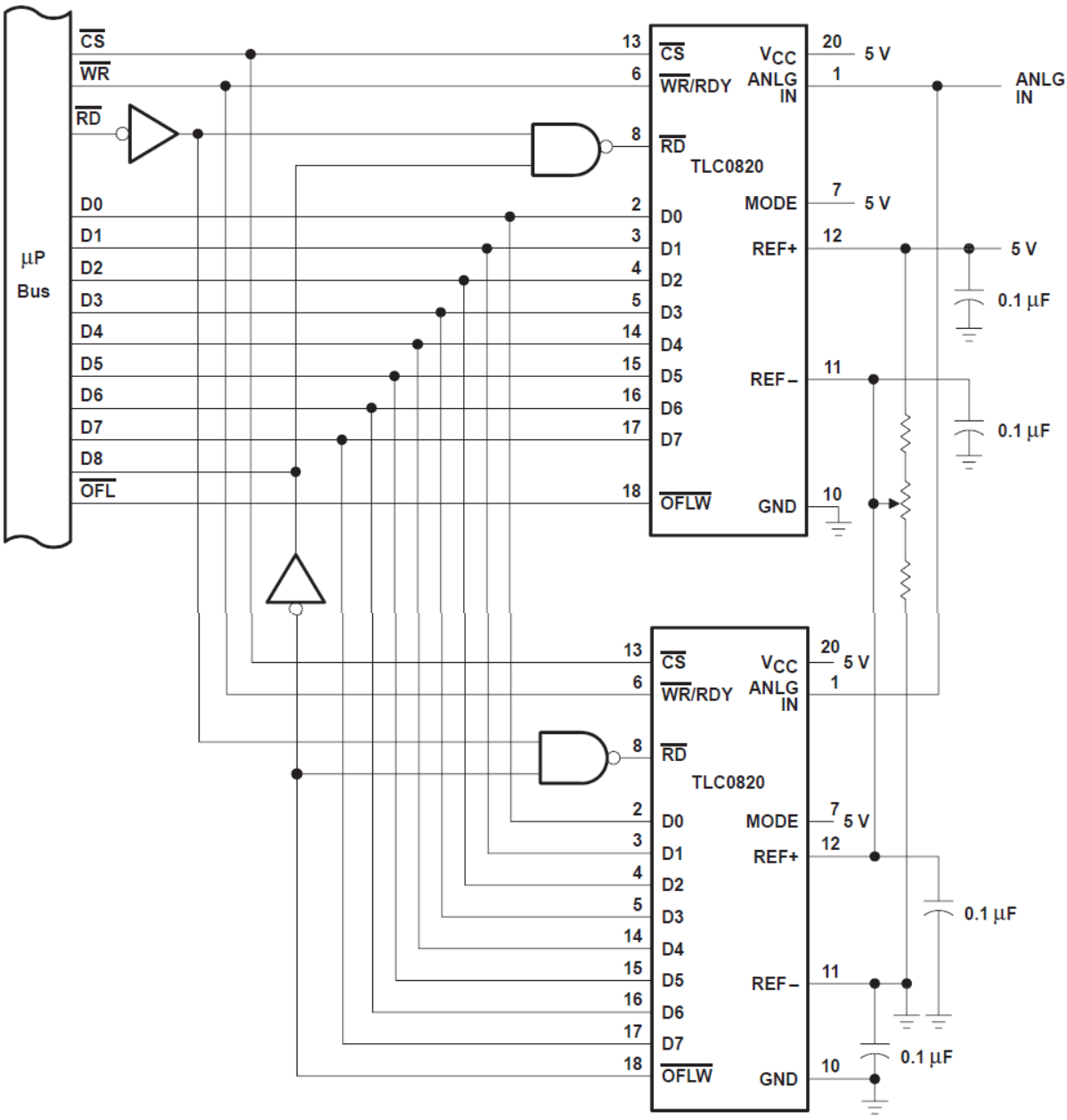


Figure 6. Configuration for 9-Bit Resolution

CONVERSOR D/A TLC7226

TLC7226C, TLC7226I, TLC7226M
QUADRUPLE 8-BIT DIGITAL-TO-ANALOG CONVERTERS

SLAS060E – JANUARY 1995 – REVISED JANUARY 2003

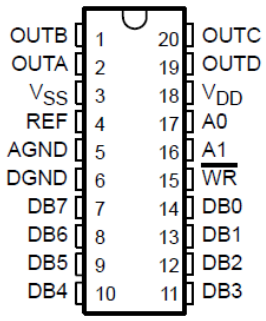
features

- Four 8-Bit D/A Converters
- Microprocessor Compatible
- TTL/CMOS Compatible
- Single Supply Operation Possible
- CMOS Technology

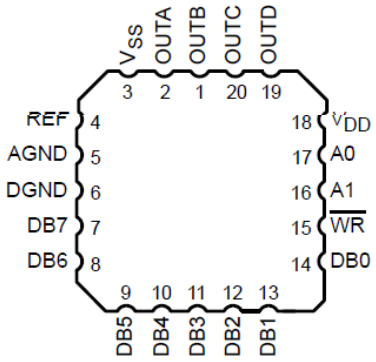
applications

- Process Control
- Automatic Test Equipment
- Automatic Calibration of Large System Parameters, e.g. Gain/Offset

DW OR N PACKAGE
(TOP VIEW)



FK PACKAGE
(TOP VIEW)



description

The TLC7226C, TLC7226I, and TLC7226M consist of four 8-bit voltage-output digital-to-analog converters (DACs) with output buffer amplifiers and interface logic on a single monolithic chip.

Separate on-chip latches are provided for each of the four DACs. Data is transferred into one of these data latches through a common 8-bit TTL/CMOS-compatible 5-V input port. Control inputs A0 and A1 determine which DAC is loaded when $\overline{WR}$ goes low. The control logic is speed compatible with most 8-bit microprocessors.

Each DAC includes an output buffer amplifier capable of sourcing up to 5 mA of output current.

The TLC7226 performance is specified for input reference voltages from 2 V to V_{DD} – 4 V with dual supplies. The voltage mode configuration of the DACs allows the TLC7226 to be operated from a single power supply rail at a reference of 10 V.

The TLC7226 is fabricated in a LinBiCMOS™ process that has been specifically developed to allow high-speed digital logic circuits and precision analog circuits to be integrated on the same chip. The TLC7226 has a common 8-bit data bus with individual DAC latches. This provides a versatile control architecture for simple interface to microprocessors. All latch-enable signals are level triggered.

Combining four DACs, four operational amplifiers, and interface logic into either a 0.3-inch wide, 20-terminal dual-in-line IC (DIP) or a small 20-terminal small-outline IC (SOIC) allows a dramatic reduction in board space requirements and offers increased reliability in systems using multiple converters. The Leadless Ceramic Chip Carrier (LCCC) package provides for operation at military temperature range. The pinout is aimed at optimizing board layout with all of the analog inputs and outputs at one end of the package and all of the digital inputs at the other.

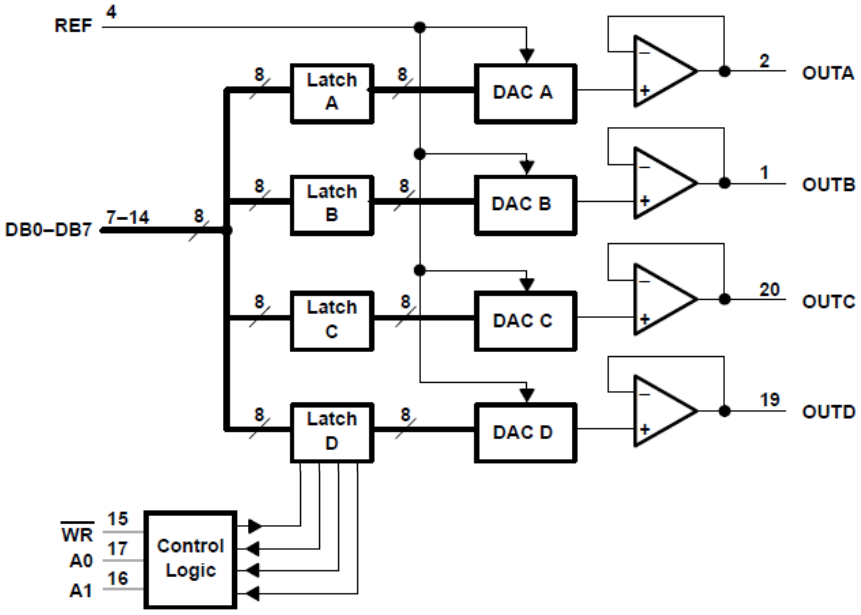
description (continued)

The TLC7226C is characterized for operation from 0°C to 70°C. The TLC7226I is characterized for operation from –25°C to 85°C. The TLC7226M is characterized for operation from –55°C to 125°C.

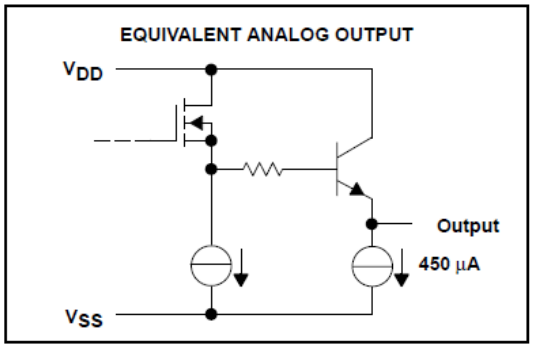
AVAILABLE OPTIONS

T_A	PACKAGE		
	SMALL OUTLINE (DW)	PLASTIC DIP (N)	LCCC (FK)
0°C to 70°C	TLC7226CDW	TLC7226CN	—
–25°C to 85°C	TLC7226IDW	TLC7226IN	—
–55°C to 125°C	—	—	TLC7226MFKB

functional block diagram



schematic of outputs



Terminal Functions

TERMINAL NAME	TERMINAL NO.†	I/O	DESCRIPTION
AGND	5		Analog ground. AGND is the reference and return terminal for the analog signals and supply.
A0, A1	17, 16	I	DAC select inputs. The combination of high or low levels select either DACA, DACB, DACC, or DACD.
DGND	6		Digital ground. DGND is the reference and return terminal for the digital signals and supply.
DB0–DB7	14–7	I	Digital DAC data inputs. DB0–DB7 are the input digital data used for conversion.
OUTA	2	O	DACA output. OUTA is the analog output of DACA.
OUTB	1	O	DACB output. OUTB is the analog output of DACB.
OUTC	20	O	DACC output. OUTC is the analog output of DACC.
OUTD	19	O	DACD output. OUTD is the analog output of DACD.
REF	4	I	Voltage reference input. The voltage level on REF determines the full scale analog output.
V_{DD}	18		Positive supply voltage input terminal
V_{SS}	3		Negative supply voltage input terminal
$\overline{WR}$	15	I	Write input. $\overline{WR}$ selects DAC transparency or latch mode. The selected input latch is transparent when $\overline{WR}$ is low.

† Terminal numbers shown are for the DW, N, and FK packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{DD}: AGND or DGND ..... –0.3 V to 17 V
V_{SS}‡ ..... –0.3 V to 24 V
Supply voltage range, V_{SS}: AGND or DGND ..... –7 V to 0.3 V
Voltage range between AGND and DGND ..... –17 V to 17 V
Input voltage range, V_I (to DGND) ..... –0.3 V to V_{DD} + 0.3 V
Reference voltage range: V_{ref} (to AGND) ..... –0.3 V to V_{DD}
V_{ref} (to V_{SS}) ..... –0.3 V to 20 V
Output voltage range, V_O (to AGND) (see Note 1) ..... V_{SS} to V_{DD}
Continuous total power dissipation at (or below) T_A = 25°C (see Note 2) ..... 500 mW
Operating free-air temperature range, T_A: C suffix ..... 0°C to 70°C
E suffix ..... –25°C to 85°C
M suffix ..... –55°C to 125°C
Storage temperature range, T_{stg} ..... –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: DW or N packages ..... 260°C
Case temperature for 10 seconds: FK package ..... 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

‡ The V_{SS} terminal is connected to the substrate and must be tied to the most negative supply voltage applied to the device.

NOTES: 1. Output voltages may be shorted to AGND provided that the power dissipation of the package is not exceeded. Typically short circuit current to AGND is 60 mA.
2. For operation above T_A = 75°C, derate linearly at the rate of 2 mW/°C.

recommended operating conditions

		MIN	MAX	UNIT
Supply voltage, V_{DD}		11.4	16.5	V
Supply voltage, V_{SS}		–5.5	0	V
High-level input voltage, V_{IH}		2		V
Low-level input voltage, V_{IL}			0.8	V
Reference voltage, V_{ref}		0	V_{DD}–4	V
Load resistance, R_L		2		kΩ
Setup time, address valid before $\overline{WR}\downarrow$, $t_{su(AW)}$ (see Figure 6)	V_{DD} = 11.4 V to 16.5 V	*0		ns
Setup time, data valid before $\overline{WR}\uparrow$, $t_{su(DW)}$ (see Figure 6)	V_{DD} = 11.4 V to 16.5 V	*45		ns
Hold time, address valid before $\overline{WR}\uparrow$, $t_{h(AW)}$ (see Figure 6)	V_{DD} = 11.4 V to 16.5 V	*0		ns
Hold time, data valid before $\overline{WR}\uparrow$, $t_{h(DW)}$ (see Figure 6)	V_{DD} = 11.4 V to 16.5 V	*10		ns
Pulse duration, $\overline{WR}$ low, t_w (see Figure 6)	V_{DD} = 11.4 V to 16.5 V	*50		ns
Operating free-air temperature, T_A	C suffix	0	70	°C
	I suffix	–25	85	
	M suffix	–55	125	

* This parameter is not tested for M suffix devices.

electrical characteristics over recommended operating free-air temperature range

dual power supply over recommended power supply and reference voltage ranges, AGND = DGND = 0 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_I	Input current, digital		V_I = 0 V or V_{DD}				±1	μA
$I_{(DD)}$	Supply current		V_I = 0.8 V or 2.4 V, V_{SS} = – 5 V,	V_{DD} = 16.5 V, No load		6	16	mA
$I_{(SS)}$	Supply current		V_I = 0.8 V or 2.4 V,	No load		4	10	mA
$r_{i(ref)}$	Reference input resistance				2	4		kΩ
	Power supply sensitivity		ΔV_{DD} = ±5%				0.01	%/%
C_i	Input capacitance	REF input	All 0s loaded	C and I suffix	65			pF
				M suffix	*30			
			All 1s loaded				*300	
		Digital inputs		C and I suffix			8	
				M suffix			*12	

* This parameter is not tested for M suffix devices.

operating characteristics over recommended operating free-air temperature range

dual power supply over recommended power supply and reference voltage ranges, AGND = DGND = 0 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Slew rate			*2.5			V•µs
Settling time to 1/2 LSB	Positive full scale	V_{ref} = 10 V			*5	µs
	Negative full scale				*7	
Resolution				8		bits
Total unadjusted error		V_{DD} = 15 V ±5%, V_{ref} = 10 V			±2	LSB
Linearity error	Differential/integral				±1	LSB
Full-scale error					±2	LSB
Gain error				±0.25		LSB
Temperature coefficient of gain	Full scale	V_{DD} = 14 V to 16.5 V, V_{ref} = 10 V		±20		ppm/°C
	Zero-code error			±50		µV/°C
Zero-code error				±20	±80	mV
Digital crosstalk glitch impulse area		V_{ref} = 0		50		nV•s

* This parameter is not tested for M suffix devices.

single power supply, V_{DD} = 14.25 V to 15.75 V, V_{SS} = AGND = DGND = 0 V, V_{ref} = 10 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply current, I_{DD}		V_I = 0.8 V or 2.4 V, No load		5	13	mA
Slew rate			*2			V•µs
Settling time to 1/2 LSB	Positive full scale				*5	µs
	Negative full scale				*20	
Resolution				8		bits
Total unadjusted error					±2	LSB
Full-scale error					±2	LSB
Temperature coefficient of gain	Full scale	V_{DD} = 14 V to 16.5 V, V_{ref} = 10 V		±20		ppm/°C
	Zero-code error			±50		µV/°C
Linearity error	Differential				±1	LSB
Digital crosstalk-glitch impulse area				50		nV•s

* This parameter is not tested for M suffix devices.

MODULADOR XR-2206

EXAR ...the analog plus company™

XR-2206
Monolithic
Function Generator

June 1997-3

FEATURES

- Low-Sine Wave Distortion, 0.5%, Typical
- Excellent Temperature Stability, 20ppm/°C, Typ.
- Wide Sweep Range, 2000:1, Typical
- Low-Supply Sensitivity, 0.01%V, Typ.
- Linear Amplitude Modulation
- TTL Compatible FSK Controls
- Wide Supply Range, 10V to 26V
- Adjustable Duty Cycle, 1% TO 99%

APPLICATIONS

- Waveform Generation
- Sweep Generation
- AM/FM Generation
- V/F Conversion
- FSK Generation
- Phase-Locked Loops (VCO)

GENERAL DESCRIPTION

The XR-2206 is a monolithic function generator integrated circuit capable of producing high quality sine, square, triangle, ramp, and pulse waveforms of high-stability and accuracy. The output waveforms can be both amplitude and frequency modulated by an external voltage. Frequency of operation can be selected externally over a range of 0.01Hz to more than 1MHz.

The circuit is ideally suited for communications, instrumentation, and function generator applications requiring sinusoidal tone, AM, FM, or FSK generation. It has a typical drift specification of 20ppm/°C. The oscillator frequency can be linearly swept over a 2000:1 frequency range with an external control voltage, while maintaining low distortion.

ORDERING INFORMATION

Part No.	Package	Operating Temperature Range
XR-2206M	16 Lead 300 Mil CDIP	-55°C to +125°C
XR-2206P	16 Lead 300 Mil PDIP	–40°C to +85°C
XR-2206CP	16 Lead 300 Mil PDIP	0°C to +70°C
XR-2206D	16 Lead 300 Mil JEDEC SOIC	0°C to +70°C

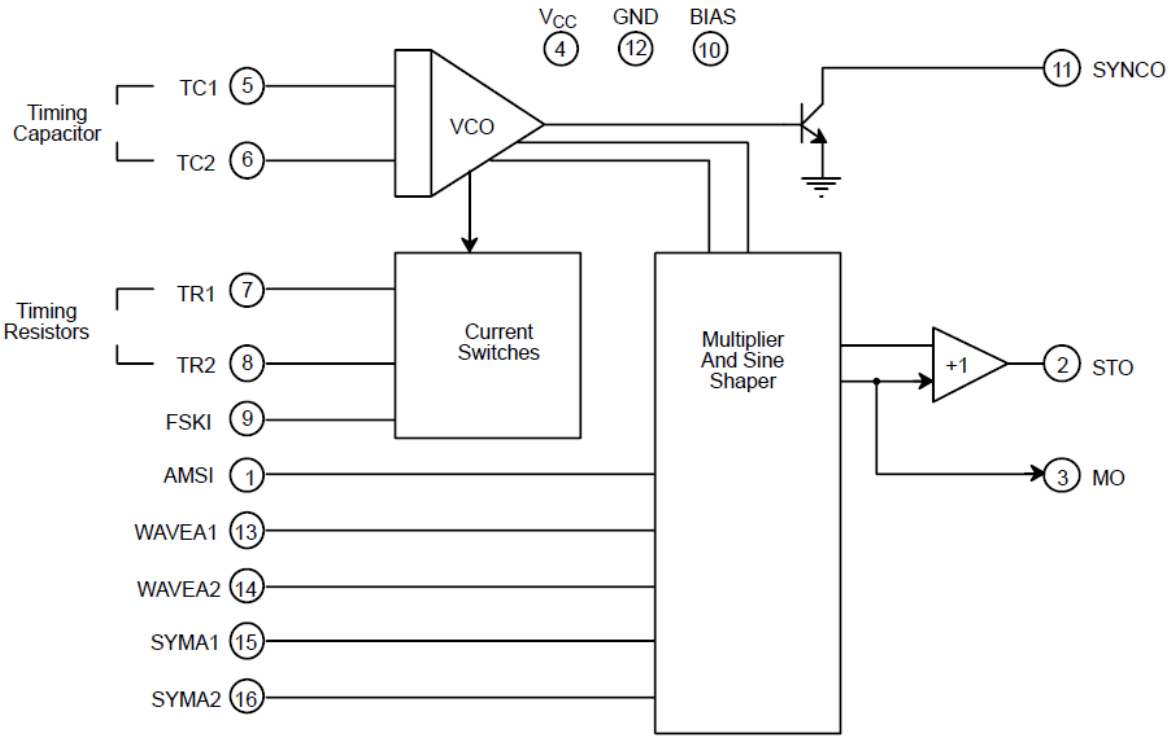
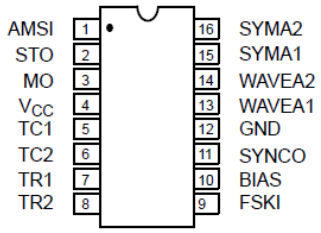
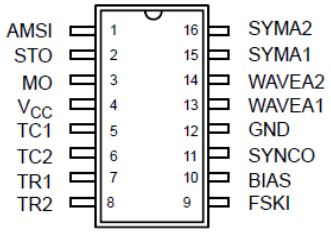


Figure 1. XR-2206 Block Diagram



16 Lead PDIP, CDIP (0.300")



16 Lead SOIC (Jedec, 0.300")

PIN DESCRIPTION

Pin #	Symbol	Type	Description
1	AMSI	I	**Amplitude Modulating Signal Input.**
2	STO	O	**Sine or Triangle Wave Output.**
3	MO	O	**Multiplier Output.**
4	V_{CC}		**Positive Power Supply.**
5	TC1	I	**Timing Capacitor Input.**
6	TC2	I	**Timing Capacitor Input.**
7	TR1	O	**Timing Resistor 1 Output.**
8	TR2	O	**Timing Resistor 2 Output.**
9	FSKI	I	**Frequency Shift Keying Input.**
10	BIAS	O	**Internal Voltage Reference.**
11	SYNCO	O	**Sync Output.** This output is a open collector and needs a pull up resistor to V_{CC}.
12	GND		**Ground pin.**
13	WAVEA1	I	**Wave Form Adjust Input 1.**
14	WAVEA2	I	**Wave Form Adjust Input 2.**
15	SYMA1	I	**Wave Symetry Adjust 1.**
16	SYMA2	I	**Wave Symetry Adjust 2.**

DC ELECTRICAL CHARACTERISTICS

Test Conditions: Test Circuit of *Figure 2* **Vcc = 12V, T_A = 25°C, C = 0.01µF, R_1 = 100kΩ, R_2 = 10kΩ, R_3 = 25kΩ** Unless Otherwise Specified. S_1 open for triangle, closed for sine wave.

Parameters	XR-2206M/P			XR-2206CP/D			Units	Conditions
	Min.	Typ.	Max.	Min.	Typ.	Max.		
General Characteristics								
Single Supply Voltage	**10**		**26**	10		26	V	
Split-Supply Voltage	**±5**		**±13**	±5		±13	V	
Supply Current		12	**17**		14	20	mA	$R_1 \geq 10k\Omega$
Oscillator Section								
Max. Operating Frequency	**0.5**	1		0.5	1		MHz	C = 1000pF, R_1 = 1kΩ
Lowest Practical Frequency		0.01			0.01		Hz	C = 50µF, R_1 = 2MΩ
Frequency Accuracy		±1	**±4**		±2		% of f_o	$f_o = 1/R_1C$
Temperature Stability Frequency		±10	**±50**		±20		ppm/°C	$0°C \leq T_A \leq 70°C$ $R_1 = R_2 = 20k\Omega$
Sine Wave Amplitude Stability[2]		4800			4800		ppm/°C	
Supply Sensitivity		0.01	**0.1**		0.01		%/V	V_{LOW} = 10V, V_{HIGH} = 20V, $R_1 = R_2 = 20k\Omega$
Sweep Range	1000:1	2000:1			2000:1		$f_H = f_L$	f_H @ R_1 = 1kΩ f_L @ R_1 = 2MΩ
Sweep Linearity								
10:1 Sweep		2			2		%	f_L = 1kHz, f_H = 10kHz
1000:1 Sweep		8			8		%	f_L = 100Hz, f_H = 100kHz
FM Distortion		0.1			0.1		%	±10% Deviation
Recommended Timing Components								
Timing Capacitor: C	**0.001**		100	0.001		100	µF	*Figure 5*
Timing Resistors: R_1 & R_2	**1**		2000	1		2000	kΩ	
Triangle Sine Wave Output[1]								*Figure 3*
Triangle Amplitude		160			160		mV/kΩ	*Figure 2*, S_1 Open
Sine Wave Amplitude	**40**	60	80		60		mV/kΩ	*Figure 2*, S_1 Closed
Max. Output Swing		6			6		Vp-p	
Output Impedance		600			600		Ω	
Triangle Linearity		1			1		%	
Amplitude Stability		0.5			0.5		dB	For 1000:1 Sweep
Sine Wave Distortion								
Without Adjustment		2.5			2.5		%	R_1 = 30kΩ
With Adjustment		0.4	**1.0**		0.5	1.5	%	See *Figure 7* and *Figure 8*

Notes

[1] Output amplitude is directly proportional to the resistance, R_3, on Pin 3. See Figure 3.

[2] For maximum amplitude stability, R_3 should be a positive temperature coefficient resistor.

***Bold face parameters** are covered by production test and guaranteed over operating temperature range.*

DC ELECTRICAL CHARACTERISTICS (CONT'D)

Parameters	XR-2206M/P			XR-2206CP/D			Units	Conditions
	Min.	Typ.	Max.	Min.	Typ.	Max.		
Amplitude Modulation								
Input Impedance	50	100		50	100		kΩ	
Modulation Range		100			100		%	
Carrier Suppression		55			55		dB	
Linearity		2			2		%	For 95% modulation
Square-Wave Output								
Amplitude		12			12		Vp-p	Measured at Pin 11.
Rise Time		250			250		ns	C_L = 10pF
Fall Time		50			50		ns	C_L = 10pF
Saturation Voltage		0.2	**0.4**		0.2	0.6	V	I_L = 2mA
Leakage Current		0.1	**20**		0.1	100	μA	V_{CC} = 26V
FSK Keying Level (Pin 9)	0.8	1.4	**2.4**	0.8	1.4	2.4	V	See section on circuit controls
Reference Bypass Voltage	2.9	3.1	**3.3**	2.5	3	3.5	V	Measured at Pin 10.

Notes
[1] Output amplitude is directly proportional to the resistance, R_3, on Pin 3. See Figure 3.
[2] For maximum amplitude stability, R_3 should be a positive temperature coefficient resistor.
***Bold face parameters** are covered by production test and guaranteed over operating temperature range.*

Specifications are subject to change without notice

ABSOLUTE MAXIMUM RATINGS

Power Supply 26V
Power Dissipation 750mW
Derate Above 25°C ..... 5mW/°C
Total Timing Current 6mA
Storage Temperature ..... -65°C to +150°C

SYSTEM DESCRIPTION

The XR-2206 is comprised of four functional blocks; a voltage-controlled oscillator (VCO), an analog multiplier and sine-shaper; a unity gain buffer amplifier; and a set of current switches.

The VCO produces an output frequency proportional to an input current, which is set by a resistor from the timing terminals to ground. With two timing pins, two discrete output frequencies can be independently produced for FSK generation applications by using the FSK input control pin. This input controls the current switches which select one of the timing resistor currents, and routes it to the VCO.

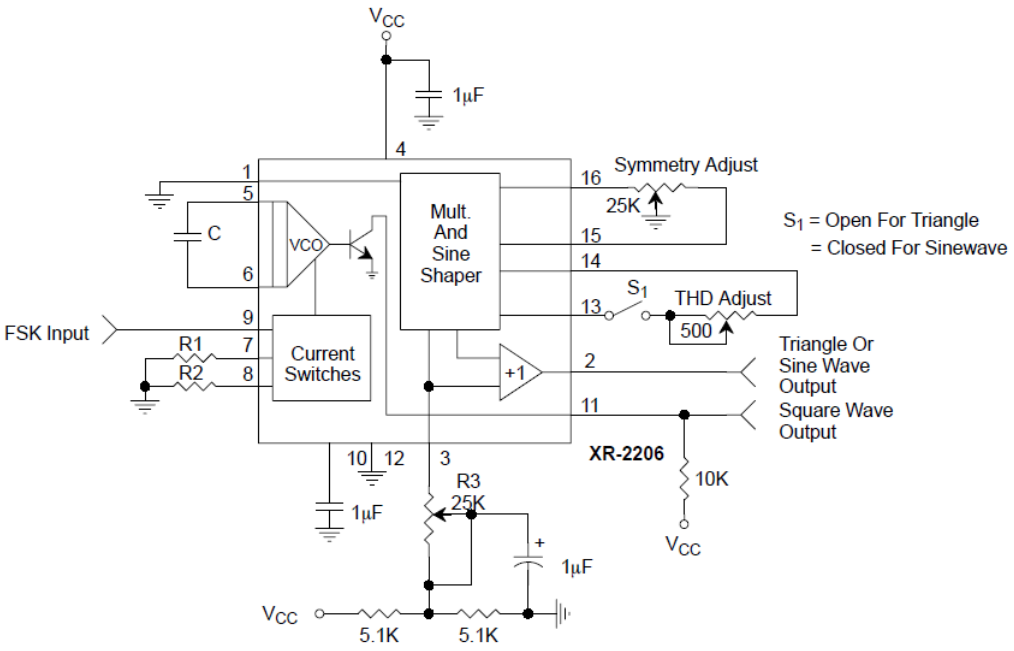


Figure 2. Basic Test Circuit

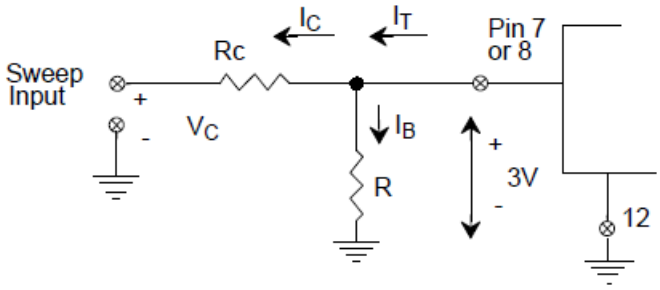


Figure 10. Circuit Connection for Frequency Sweep.

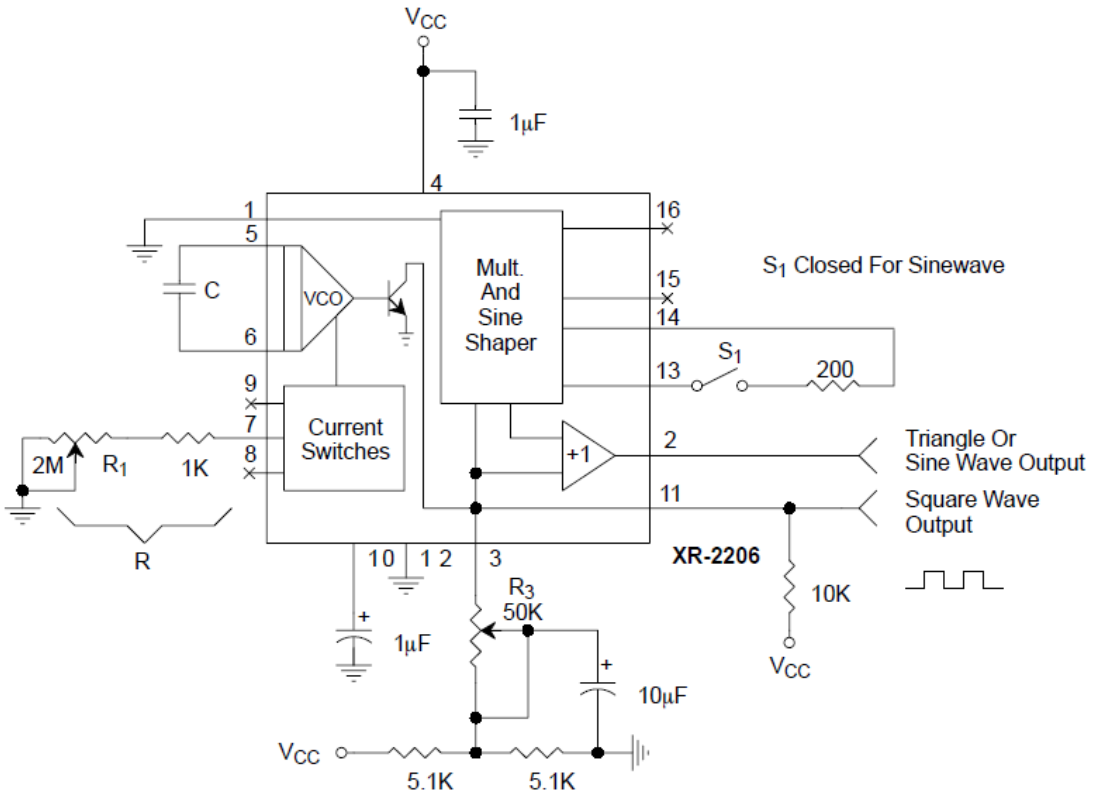


Figure 11. Circuit tor Sine Wave Generation without External Adjustment. (See *Figure 3* for Choice of R_3)

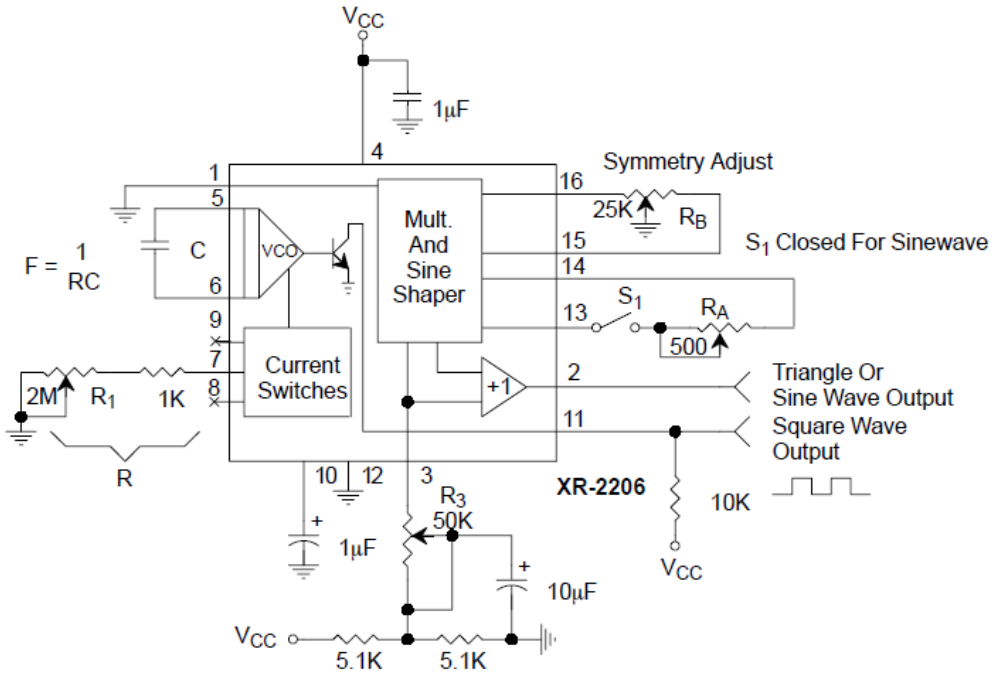


Figure 12. Circuit for Sine Wave Generation with Minimum Harmonic Distortion. (R_3 Determines Output Swing - See *Figure 3*)

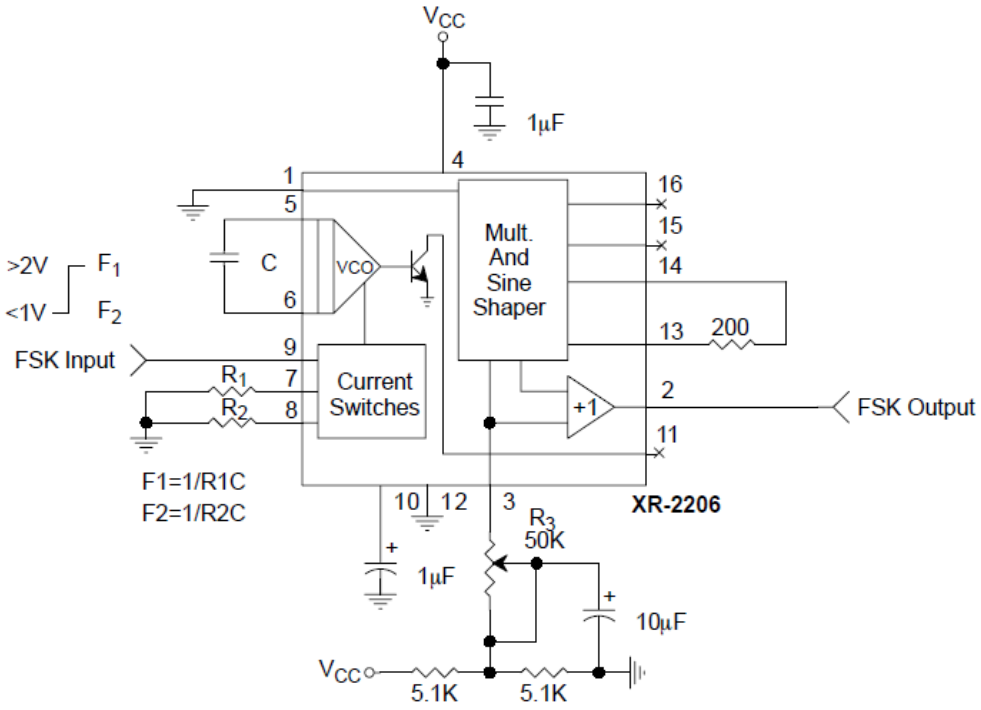


Figure 13. Sinusoidal FSK Generator

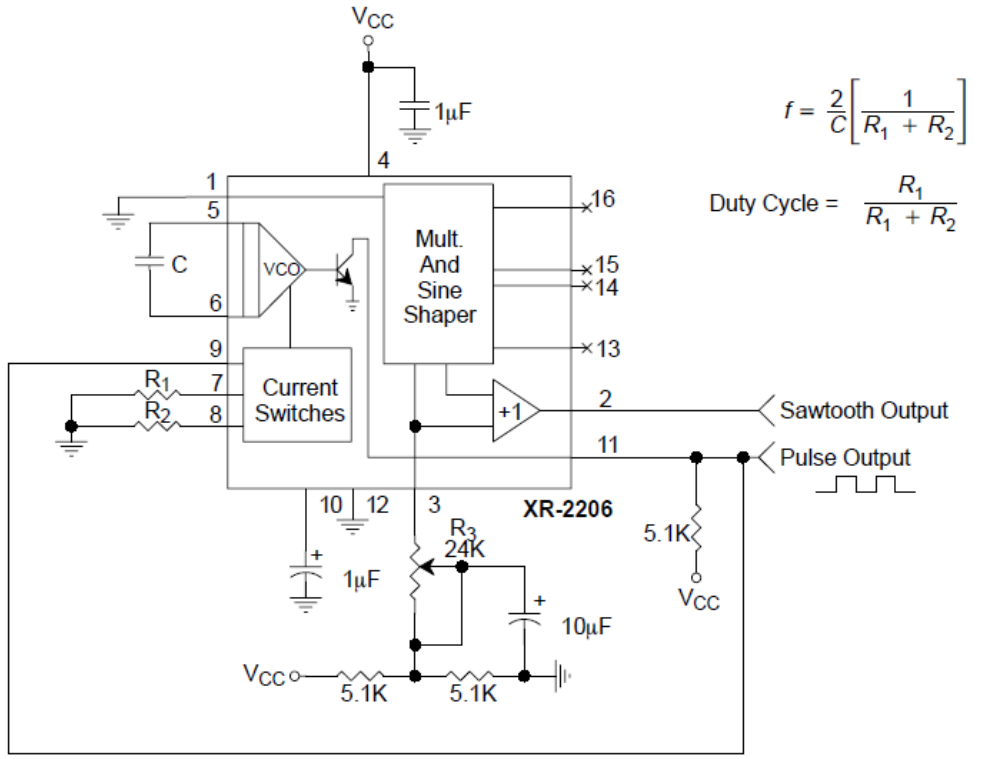


Figure 14. Circuit for Pulse and Ramp Generation.

DdDEMODULADOR XR-2211

EXAR ...the analog plus company™

XR-2211
FSK Demodulator/
Tone Decoder

June 1997-3

FEATURES

- Wide Frequency Range, 0.01Hz to 300kHz
- Wide Supply Voltage Range, 4.5V to 20V
- HCMOS/TTL/Logic Compatibility
- FSK Demodulation, with Carrier Detection
- Wide Dynamic Range, 10mV to 3V rms
- Adjustable Tracking Range, ±1% to 80%
- Excellent Temp. Stability, ±50ppm/°C, max.

APPLICATIONS

- Caller Identification Delivery
- FSK Demodulation
- Data Synchronization
- Tone Decoding
- FM Detection
- Carrier Detection

GENERAL DESCRIPTION

The XR-2211 is a monolithic phase-locked loop (PLL) system especially designed for data communications applications. It is particularly suited for FSK modem applications. It operates over a wide supply voltage range of 4.5 to 20V and a wide frequency range of 0.01Hz to 300kHz. It can accommodate analog signals between 10mV and 3V, and can interface with conventional DTL, TTL, and ECL logic families. The circuit consists of a basic PLL for tracking an input signal within the pass band, a quadrature phase detector which provides carrier detection, and an FSK voltage comparator which provides FSK demodulation. External components are used to independently set center frequency, bandwidth, and output delay. An internal voltage reference proportional to the power supply is provided at an output pin.

The XR-2211 is available in 14 pin packages specified for military and industrial temperature ranges.

ORDERING INFORMATION

Part No.	Package	Operating Temperature Range
XR-2211M	14 Pin CDIP (0.300")	-55°C to +125°C
XR-2211N	14 Pin CDIP (0.300")	-40°C to +85°C
XR-2211P	14 Pin PDIP (0.300")	-40°C to +85°C
XR-2211ID	14 Lead SOIC (Jedec, 0.150")	-40°C to +85°C

BLOCK DIAGRAM

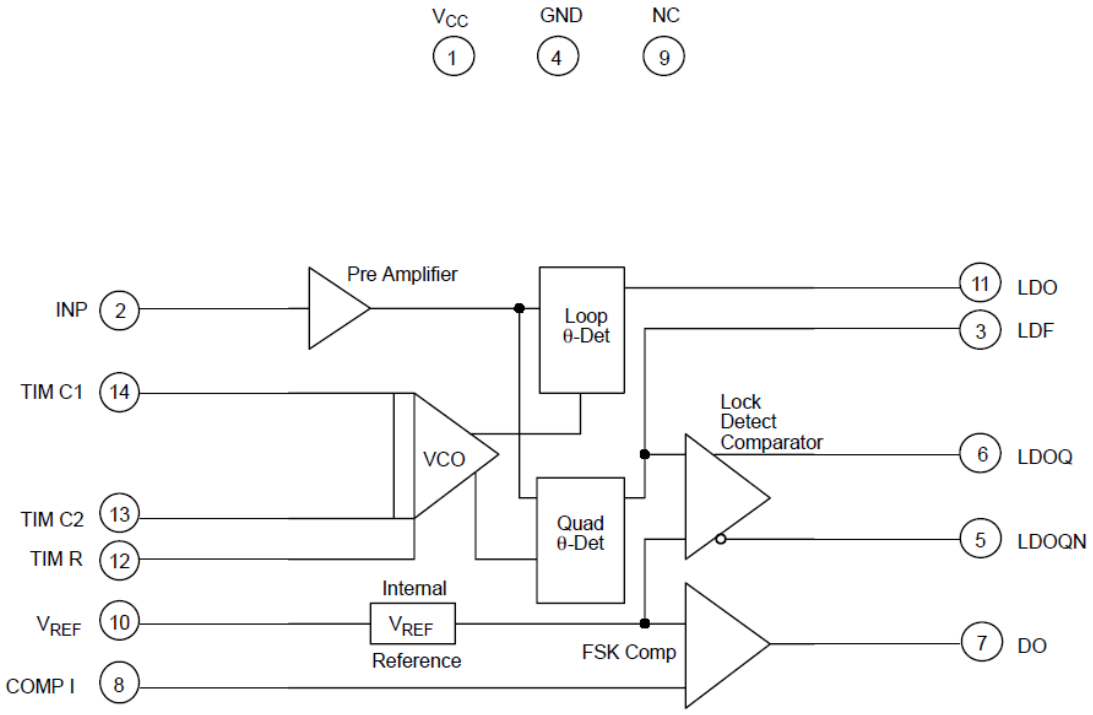
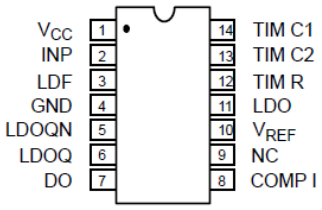
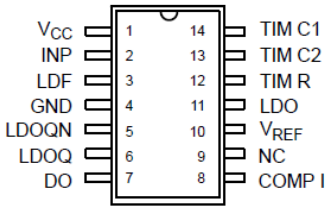


Figure 1. XR-2211 Block Diagram

PIN CONFIGURATION



14 Lead CDIP, PDIP (0.300")



14 Lead SOIC (Jedec, 0.150")

PIN DESCRIPTION

Pin #	Symbol	Type	Description
1	V_{CC}		**Positive Power Supply.**
2	INP	I	**Receive Analog Input.**
3	LDF	O	**Lock Detect Filter.**
4	GND		**Ground Pin.**
5	LDOQN	O	**Lock Detect Output Not.** This output will be low if the VCO is in the capture range.
6	LDOQ	O	**Lock Detect Output.** This output will be high if the VCO is in the capture range.
7	DO	O	**Data Output.** Decoded FSK output.
8	COMP I	I	**FSK Comparator Input.**
9	NC		**Not Connected.**
10	V_{REF}	O	**Internal Voltage Reference.** The value of V_{REF} is V_{CC}/2 - 650mV.
11	LDO	O	**Loop Detect Output.** This output provides the result of the quadrature phase detection.
12	TIM R	I	**Timing Resistor Input.** This pin connects to the timing resistor of the VCO.
13	TIM C2	I	**Timing Capacitor Input.** The timing capacitor connects between this pin and pin 14.
14	TIM C1	I	**Timing Capacitor Input.** The timing capacitor connects between this pin and pin 13.

ELECTRICAL CHARACTERISTICS
Test Conditions: V_{CC} = 12V, T_A = +25°C, R_O = 30KΩ, C_O = 0.033μF, unless otherwise specified.

Parameter	Min.	Typ.	Max.	Unit	Conditions
General					
Supply Voltage	**4.5**		**20**	V	
Supply Current		4	**7**	mA	$R_0 \geq$ 10KΩ. See *Figure 4.*
Oscillator Section					
Frequency Accuracy		±1	**±3**	%	Deviation from $f_O = 1/R_0 C_0$
Frequency Stability					
Temperature		±20	±50	ppm/°C	See *Figure 8.*
Power Supply		0.05	**0.5**	%/V	V_{CC} = 12 ±1V. See *Figure 7.*
		0.2		%/V	V_{CC} = ± 5V. See *Figure 7.*
Upper Frequency Limit	**100**	300		kHz	R_0 = 8.2KΩ, C_0 = 400pF
Lowest Practical Operating Frequency			0.01	Hz	R_0 = 2MΩ, C_0 = 50μF
Timing Resistor, R_0 - See *Figure 5*					
Operating Range	**5**		2000	KΩ	
Recommended Range	5			KΩ	See *Figure 7* and *Figure 8.*
Loop Phase Dectector Section					
Peak Output Current	**±150**	±200	**±300**	μA	Measured at Pin 11
Output Offset Current		1		μA	
Output Impedance		1		MΩ	
Maximum Swing	**±4**	± 5		V	Referenced to Pin 10
Quadrature Phase Detector					Measured at Pin 3
Peak Output Current	**100**	300		μA	
Output Impedance		1		MΩ	
Maximum Swing		11		V_{PP}	
Input Preampt Section					Measured at Pin 2
Input Impedance		20		KΩ	
Input Signal					
Voltage Required to Cause Limiting		2	10	mV rms	

Notes
Parameters are guaranteed over the recommended operating conditions, but are not 100% tested in production.
***Bold face parameters** are covered by production test and guaranteed over operating temperature range.*

DC ELECTRICAL CHARACTERISTICS (CONT'D)

Test Conditions: V_{CC} = 12V, T_A = +25°C, R_O = 30KΩ, C_O = 0.033μF, unless otherwise specified.

Parameter	Min.	Typ.	Max.	Unit	Conditions
Voltage Comparator Section					
Input Impedance		2		MΩ	Measured at Pins 3 and 8
Input Bias Current		100		nA	
Voltage Gain	55	70		dB	R_L = 5.1KΩ
Output Voltage Low		300	**500**	mV	I_C = 3mA
Output Leakage Current		0.01	**10**	μA	V_O = 20V
Internal Reference					
Voltage Level	**4.9**	5.3	**5.7**	V	Measured at Pin 10
Output Impedance		100		Ω	AC Small Signal
Maximum Source Current		80		μA	

Notes
Parameters are guaranteed over the recommended operating conditions, but are not 100% tested in production.
***Bold face parameters** are covered by production test and guaranteed over operating temperature range.*

Specifications are subject to change without notice

ABSOLUTE MAXIMUM RATINGS

Power Supply 20V
Input Signal Level ..... 3V rms
Power Dissipation 900mW

Package Power Dissipation Ratings
CDIP 750mW
Derate Above T_A = 25°C ..... 8mW/°C
PDIP 800mW
Derate Above T_A = 25°C ..... 60mW/°C
SOIC 390mW
Derate Above T_A = 25°C ..... 5mW/°C

SYSTEM DESCRIPTION

The main PLL within the XR-2211 is constructed from an input preamplifier, analog multiplier used as a phase detector and a precision voltage controlled oscillator (VCO). The preamplifier is used as a limiter such that input signals above typically 10mV rms are amplified to a constant high level signal. The multiplying-type phase detector acts as a digital exclusive or gate. Its output (unfiltered) produces sum and difference frequencies of the input and the VCO output. The VCO is actually a current controlled oscillator with its normal input current (f_O) set by a resistor (R_0) to ground and its driving current with a resistor (R_1) from the phase detector.

The output of the phase detector produces sum and difference of the input and the VCO frequencies (internally connected). When in lock, these frequencies are f_{IN}+ f_{VCO} (2 times f_{IN} when in lock) and f_{IN} - f_{VCO} (0Hz when lock). By adding a capacitor to the phase detector output, the 2 times f_{IN} component is reduced, leaving a DC voltage that represents the phase difference between the two frequencies. This closes the loop and allows the VCO to track the input frequency.

The FSK comparator is used to determine if the VCO is driven above or below the center frequency (FSK comparator). This will produce both active high and active low outputs to indicate when the main PLL is in lock (quadrature phase detector and lock detector comparator).

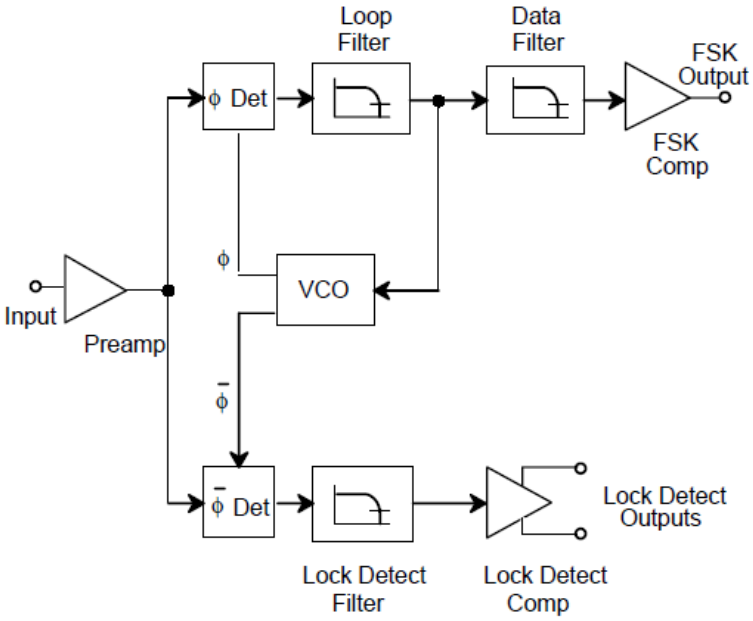


Figure 2. Functional Block Diagram of a Tone and FSK Decoding System Using XR-2211

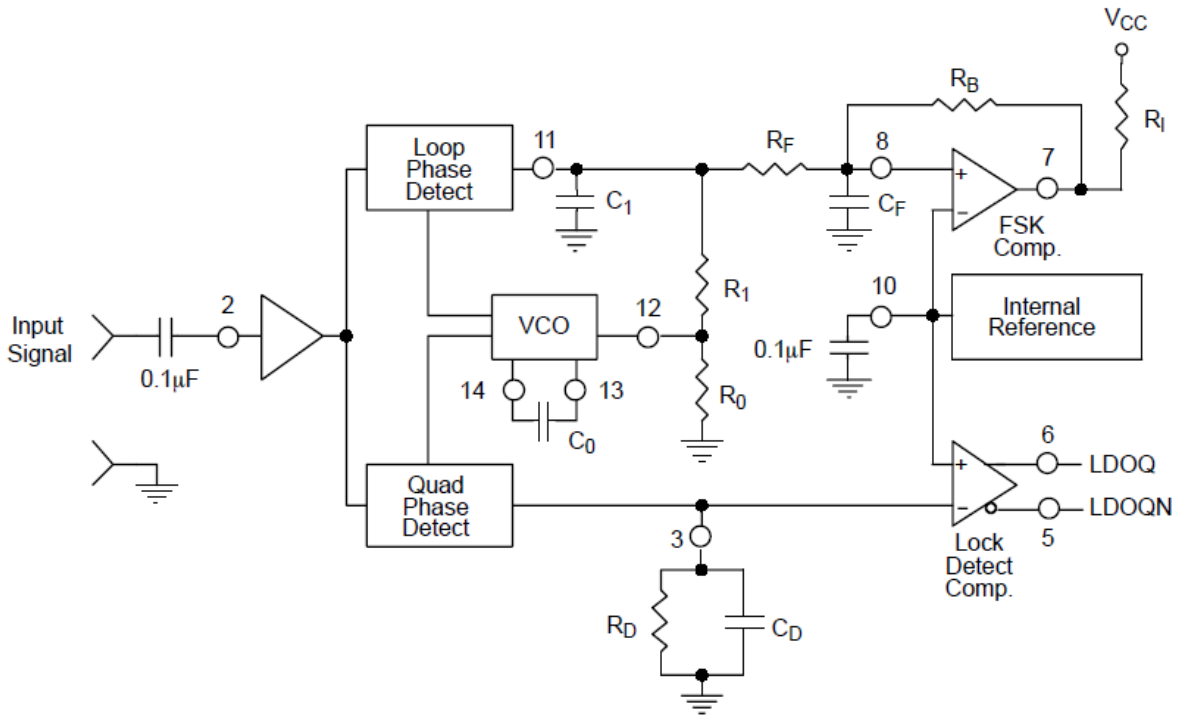


Figure 3. Generalized Circuit Connection for FSK and Tone Detection

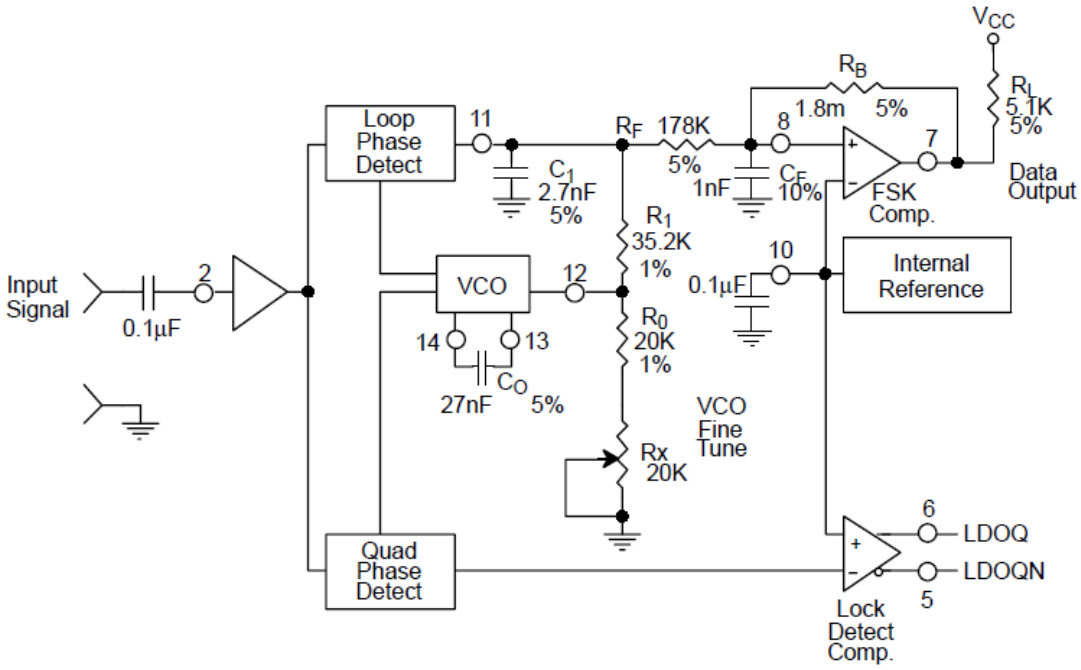


Figure 10. Circuit Connection for FSK Decoding of Caller Identification Signals (Bell 202 Format)

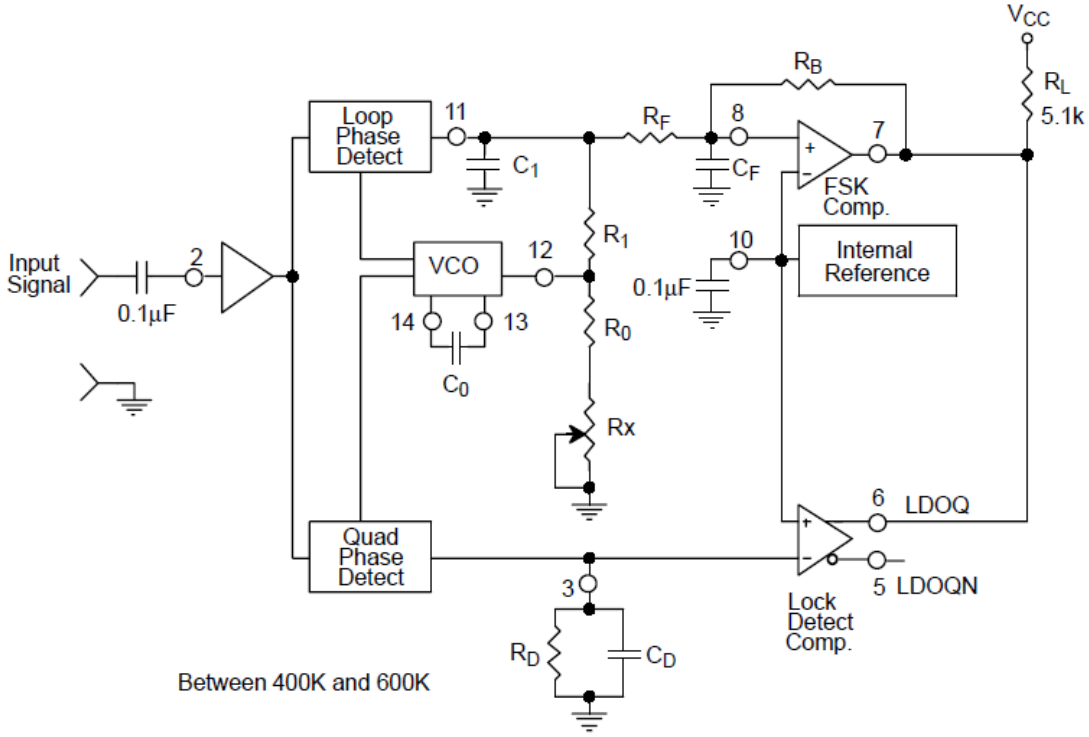


Figure 11. External Connectors for FSK Demodulation with Carrier Detect Capability

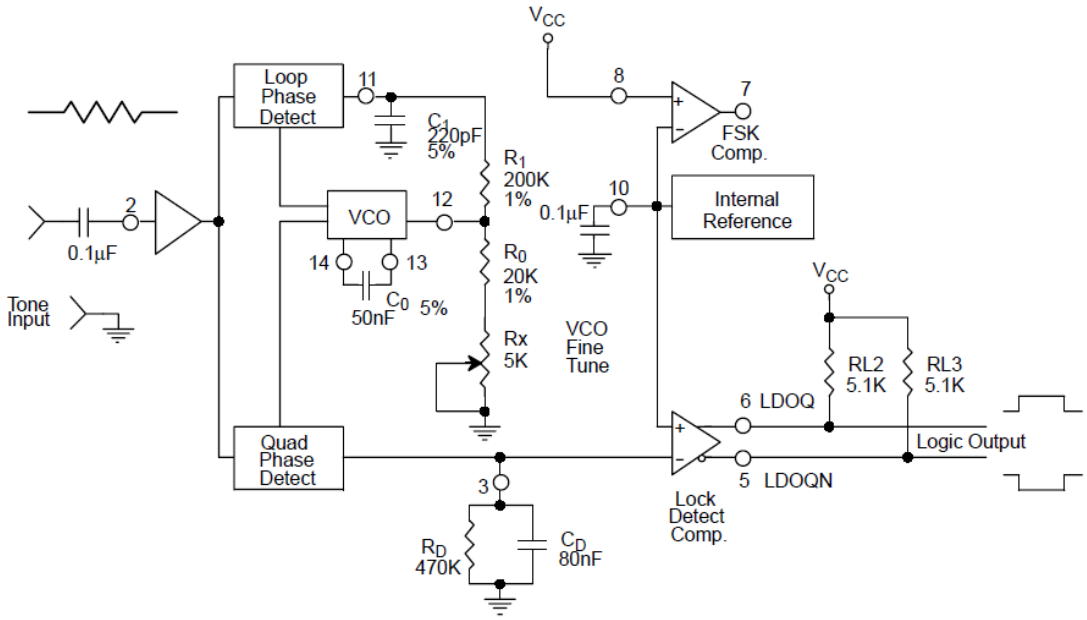


Figure 12. Circuit Connection for Tone Detection

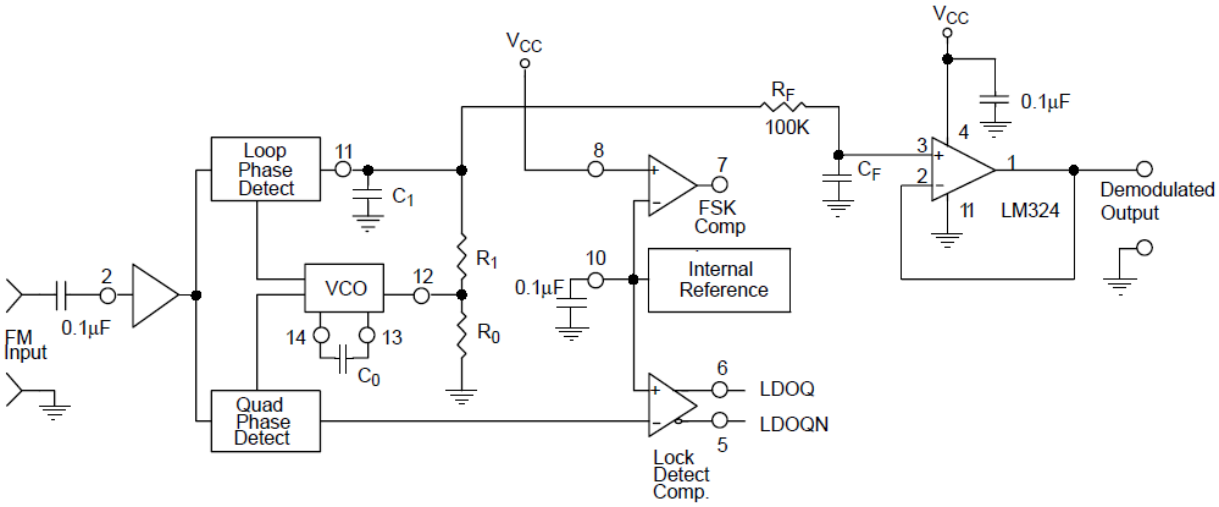


Figure 13. Linear FM Detector Using XR-2211 and an External Op Amp.
(See Section on Design Equation for Component Values.)

MICROCONTROLADOR PIC16F84

MICROCHIP

PIC16F8X

18-pin Flash/EEPROM 8-Bit Microcontrollers

Devices Included in this Data Sheet:

- PIC16F83
- PIC16F84
- PIC16CR83
- PIC16CR84
- Extended voltage range devices available (PIC16**LF**8X, PIC16**LCR**8X)

High Performance RISC CPU Features:

- Only 35 single word instructions to learn
- All instructions single cycle except for program branches which are two-cycle
- Operating speed: DC - 10 MHz clock input
  DC - 400 ns instruction cycle

Device	Program Memory (words)	Data RAM (bytes)	Data EEPROM (bytes)	Max. Freq (MHz)
PIC16F83	512 Flash	36	64	10
PIC16F84	1 K Flash	68	64	10
PIC16CR83	512 ROM	36	64	10
PIC16CR84	1 K ROM	68	64	10

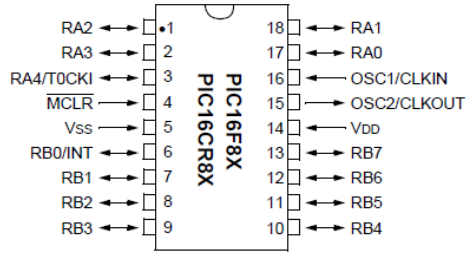
- 14-bit wide instructions
- 8-bit wide data path
- 15 special function hardware registers
- Eight-level deep hardware stack
- Direct, indirect and relative addressing modes
- Four interrupt sources:
  - External RB0/INT pin
  - TMR0 timer overflow
  - PORTB<7:4> interrupt on change
  - Data EEPROM write complete
- 1000 erase/write cycles Flash program memory
- 10,000,000 erase/write cycles EEPROM data memory
- EEPROM Data Retention > 40 years

Peripheral Features:

- 13 I/O pins with individual direction control
- High current sink/source for direct LED drive
  - 25 mA sink max. per pin
  - 20 mA source max. per pin
- TMR0: 8-bit timer/counter with 8-bit programmable prescaler

Pin Diagrams

PDIP, SOIC



Special Microcontroller Features:

- In-Circuit Serial Programming (ICSP™) - via two pins (ROM devices support only Data EEPROM programming)
- Power-on Reset (POR)
- Power-up Timer (PWRT)
- Oscillator Start-up Timer (OST)
- Watchdog Timer (WDT) with its own on-chip RC oscillator for reliable operation
- Code-protection
- Power saving SLEEP mode
- Selectable oscillator options

CMOS Flash/EEPROM Technology:

- Low-power, high-speed technology
- Fully static design
- Wide operating voltage range:
  - Commercial: 2.0V to 6.0V
  - Industrial: 2.0V to 6.0V
- Low power consumption:
  - < 2 mA typical @ 5V, 4 MHz
  - 15 µA typical @ 2V, 32 kHz
  - < 1 µA typical standby current @ 2V

1.0 GENERAL DESCRIPTION

The PIC16F8X is a group in the PIC16CXX family of low-cost, high-performance, CMOS, fully-static, 8-bit microcontrollers. This group contains the following devices:

- PIC16F83
- PIC16F84
- PIC16CR83
- PIC16CR84

All PICmicro™ microcontrollers employ an advanced RISC architecture. PIC16F8X devices have enhanced core features, eight-level deep stack, and multiple internal and external interrupt sources. The separate instruction and data buses of the Harvard architecture allow a 14-bit wide instruction word with a separate 8-bit wide data bus. The two stage instruction pipeline allows all instructions to execute in a single cycle, except for program branches (which require two cycles). A total of 35 instructions (reduced instruction set) are available. Additionally, a large register set is used to achieve a very high performance level.

PIC16F8X microcontrollers typically achieve a 2:1 code compression and up to a 4:1 speed improvement (at 20 MHz) over other 8-bit microcontrollers in their class.

The PIC16F8X has up to 68 bytes of RAM, 64 bytes of Data EEPROM memory, and 13 I/O pins. A timer/counter is also available.

The PIC16CXX family has special features to reduce external components, thus reducing cost, enhancing system reliability and reducing power consumption. There are four oscillator options, of which the single pin RC oscillator provides a low-cost solution, the LP oscillator minimizes power consumption, XT is a standard crystal, and the HS is for High Speed crystals. The SLEEP (power-down) mode offers power saving. The user can wake the chip from sleep through several external and internal interrupts and resets.

A highly reliable Watchdog Timer with its own on-chip RC oscillator provides protection against software lock-up.

The devices with Flash program memory allow the same device package to be used for prototyping and production. In-circuit reprogrammability allows the code to be updated without the device being removed from the end application. This is useful in the development of many applications where the device may not be easily accessible, but the prototypes may require code updates. This is also useful for remote applications where the code may need to be updated (such as rate information).

Table 1-1 lists the features of the PIC16F8X. A simplified block diagram of the PIC16F8X is shown in Figure 3-1.

The PIC16F8X fits perfectly in applications ranging from high speed automotive and appliance motor control to low-power remote sensors, electronic locks, security devices and smart cards. The Flash/EEPROM technology makes customization of application programs (transmitter codes, motor speeds, receiver frequencies, security codes, etc.) extremely fast and convenient. The small footprint packages make this microcontroller series perfect for all applications with space limitations. Low-cost, low-power, high performance, ease-of-use and I/O flexibility make the PIC16F8X very versatile even in areas where no microcontroller use has been considered before (e.g., timer functions; serial communication; capture, compare and PWM functions; and co-processor applications).

The serial in-system programming feature (via two pins) offers flexibility of customizing the product after complete assembly and testing. This feature can be used to serialize a product, store calibration data, or program the device with the current firmware before shipping.

1.1 Family and Upward Compatibility

Those users familiar with the PIC16C5X family of microcontrollers will realize that this is an enhanced version of the PIC16C5X architecture. Please refer to Appendix A for a detailed list of enhancements. Code written for PIC16C5X devices can be easily ported to PIC16F8X devices (Appendix B).

1.2 Development Support

The PIC16CXX family is supported by a full-featured macro assembler, a software simulator, an in-circuit emulator, a low-cost development programmer and a full-featured programmer. A “C” compiler and fuzzy logic support tools are also available.

TABLE 1-1 PIC16F8X FAMILY OF DEVICES

		PIC16F83	PIC16CR83	PIC16F84	PIC16CR84
Clock	Maximum Frequency of Operation (MHz)	10	10	10	10
Memory	Flash Program Memory	512	—	1K	—
	EEPROM Program Memory	—	—	—	—
	ROM Program Memory	—	512	—	1K
	Data Memory (bytes)	36	36	68	68
	Data EEPROM (bytes)	64	64	64	64
Peripherals	Timer Module(s)	TMR0	TMR0	TMR0	TMR0
	Interrupt Sources	4	4	4	4
Features	I/O Pins	13	13	13	13
	Voltage Range (Volts)	2.0-6.0	2.0-6.0	2.0-6.0	2.0-6.0
	Packages	18-pin DIP, SOIC	18-pin DIP, SOIC	18-pin DIP, SOIC	18-pin DIP, SOIC

All PICmicro™ Family devices have Power-on Reset, selectable Watchdog Timer, selectable code protect and high I/O current capability. All PIC16F8X Family devices use serial programming with clock pin RB6 and data pin RB7.

FIGURE 3-1: PIC16F8X BLOCK DIAGRAM

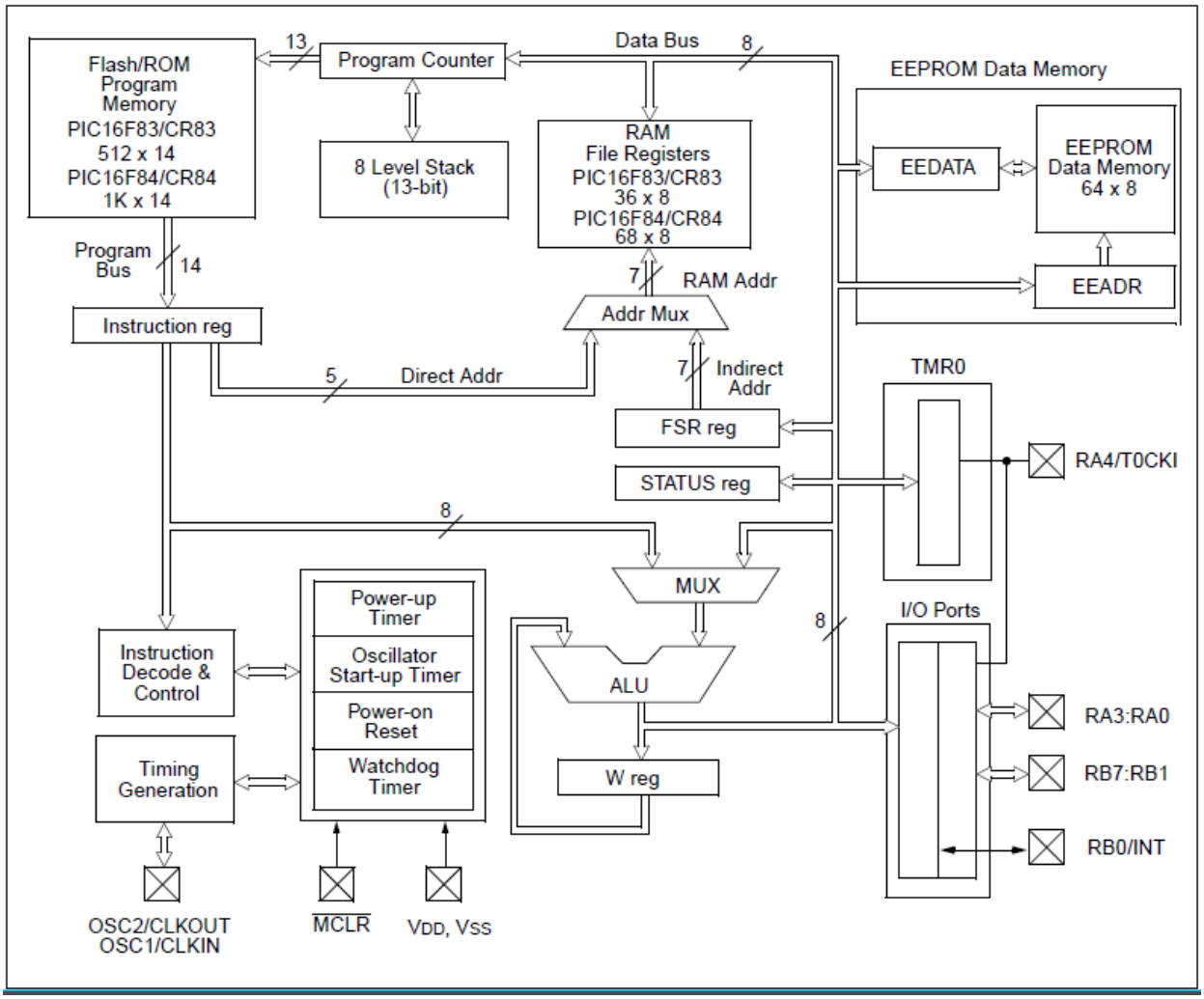


TABLE 3-1 PIC16F8X PINOUT DESCRIPTION

Pin Name	DIP No.	SOIC No.	I/O/P Type	Buffer Type	Description
OSC1/CLKIN	16	16	I	ST/CMOS (3)	Oscillator crystal input/external clock source input.
OSC2/CLKOUT	15	15	O	—	Oscillator crystal output. Connects to crystal or resonator in crystal oscillator mode. In RC mode, OSC2 pin outputs CLKOUT which has 1/4 the frequency of OSC1, and denotes the instruction cycle rate.
$\overline{MCLR}$	4	4	I/P	ST	Master clear (reset) input/programming voltage input. This pin is an active low reset to the device.
					PORTA is a bi-directional I/O port.
RA0	17	17	I/O	TTL	
RA1	18	18	I/O	TTL	
RA2	1	1	I/O	TTL	
RA3	2	2	I/O	TTL	
RA4/T0CKI	3	3	I/O	ST	Can also be selected to be the clock input to the TMR0 timer/counter. Output is open drain type.
					PORTB is a bi-directional I/O port. PORTB can be software programmed for internal weak pull-up on all inputs.
RB0/INT	6	6	I/O	TTL/ST (1)	RB0/INT can also be selected as an external interrupt pin.
RB1	7	7	I/O	TTL	
RB2	8	8	I/O	TTL	
RB3	9	9	I/O	TTL	
RB4	10	10	I/O	TTL	Interrupt on change pin.
RB5	11	11	I/O	TTL	Interrupt on change pin.
RB6	12	12	I/O	TTL/ST (2)	Interrupt on change pin. Serial programming clock.
RB7	13	13	I/O	TTL/ST (2)	Interrupt on change pin. Serial programming data.
VSS	5	5	P	—	Ground reference for logic and I/O pins.
VDD	14	14	P	—	Positive supply for logic and I/O pins.

Legend: I= input O = output I/O = Input/Output P = power
— = Not used TTL = TTL input ST = Schmitt Trigger input

Note 1: This buffer is a Schmitt Trigger input when configured as the external interrupt.
2: This buffer is a Schmitt Trigger input when used in serial programming mode.
3: This buffer is a Schmitt Trigger input when configured in RC oscillator mode and a CMOS input otherwise.

11.0 ELECTRICAL CHARACTERISTICS FOR PIC16F83 AND PIC16F84

Absolute Maximum Ratings †

Ambient temperature under bias ..... -55°C to +125°C
Storage temperature ..... -65°C to +150°C
Voltage on V_{DD} with respect to V_{SS} ..... -0.3 to +7.5V
Voltage on $\overline{MCLR}$ with respect to V_{SS} (2) ..... -0.3 to +14V
Voltage on any pin with respect to V_{SS} (except V_{DD} and $\overline{MCLR}$) ..... -0.6V to (V_{DD} + 0.6V)
Total power dissipation (1) ..... 800 mW
Maximum current out of V_{SS} pin ..... 150 mA
Maximum current into V_{DD} pin ..... 100 mA
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{DD}) ..... ± 20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{DD}) ..... ± 20 mA
Maximum output current sunk by any I/O pin ..... 25 mA
Maximum output current sourced by any I/O pin ..... 20 mA
Maximum current sunk by PORTA ..... 80 mA
Maximum current sourced by PORTA ..... 50 mA
Maximum current sunk by PORTB ..... 150 mA
Maximum current sourced by PORTB ..... 100 mA

Note 1: Power dissipation is calculated as follows: $P_{dis} = V_{DD} \times \{I_{DD} - \sum I_{OH}\} + \sum \{(V_{DD}-V_{OH}) \times I_{OH}\} + \sum(V_{OL} \times I_{OL})$

Note 2: Voltage spikes below V_{SS} at the $\overline{MCLR}$ pin, inducing currents greater than 80 mA, may cause latch-up. Thus, a series resistor of 50-100Ω should be used when applying a "low" level to the $\overline{MCLR}$ pin rather than pulling this pin directly to V_{SS}.

† NOTICE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 11-1 CROSS REFERENCE OF DEVICE SPECS FOR OSCILLATOR CONFIGURATIONS AND FREQUENCIES OF OPERATION (COMMERCIAL DEVICES)

OSC	PIC16F84-04 PIC16F83-04	PIC16F84-10 PIC16F83-10	PIC16LF84-04 PIC16LF83-04
RC	V_{DD}: 4.0V to 6.0V I_{DD}: 4.5 mA max. at 5.5V I_{PD}: 14 µA max. at 4V WDT dis Freq: 4.0 MHz max.	V_{DD}: 4.5V to 5.5V I_{DD}: 1.8 mA typ. at 5.5V I_{PD}: 1.0 µA typ. at 5.5V WDT dis Freq: 4..0 MHz max.	V_{DD}: 2.0V to 6.0V I_{DD}: 4.5 mA max. at 5.5V I_{PD}: 7.0 µA max. at 2V WDT dis Freq: 2.0 MHz max.
XT	V_{DD}: 4.0V to 6.0V I_{DD}: 4.5 mA max. at 5.5V I_{PD}: 14 µA max. at 4V WDT dis Freq: 4.0 MHz max.	V_{DD}: 4.5V to 5.5V I_{DD}: 1.8 mA typ. at 5.5V I_{PD}: 1.0 µA typ. at 5.5V WDT dis Freq: 4.0 MHz max.	V_{DD}: 2.0V to 6.0V I_{DD}: 4.5 mA max. at 5.5V I_{PD}: 7.0 µA max. at 2V WDT dis Freq: 2.0 MHz max.
HS	V_{DD}: 4.5V to 5.5V I_{DD}: 4.5 mA typ. at 5.5V I_{PD}: 1.0 µA typ. at 4.5V WDT dis Freq: 4.0 MHz max.	V_{DD}: 4.5V to 5.5V I_{DD}: 10 mA max. at 5.5V typ. I_{PD}: 1.0 µA typ. at 4.5V WDT dis Freq: 10 MHz max.	Do not use in HS mode
LP	V_{DD}: 4.0V to 6.0V I_{DD}: 48 µA typ. at 32 kHz, 2.0V I_{PD}: 0.6 µA typ. at 3.0V WDT dis Freq: 200 kHz max.	Do not use in LP mode	V_{DD}: 2.0V to 6.0V I_{DD}: 45 µA max. at 32 kHz, 2.0V I_{PD}: 7 µA max. at 2.0V WDT dis Freq: 200 kHz max.

The shaded sections indicate oscillator selections which are tested for functionality, but not for MIN/MAX specifications. It is recommended that the user select the device type that ensures the specifications required.

11.1 DC CHARACTERISTICS: PIC16F84, PIC16F83 (Commercial, Industrial)

DC Characteristics Power Supply Pins			Standard Operating Conditions (unless otherwise stated) Operating temperature 0°C ≤ TA ≤ +70°C (commercial) -40°C ≤ TA ≤ +85°C (industrial)				
Parameter No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
D001	VDD	Supply Voltage	4.0	—	6.0	V	XT, RC and LP osc configuration
D001A			4.5	—	5.5	V	HS osc configuration
D002	VDR	RAM Data Retention Voltage(1)	1.5*	—	—	V	Device in SLEEP mode
D003	VPOR	VDD start voltage to ensure internal Power-on Reset signal	—	VSS	—	V	See section on Power-on Reset for details
D004	SVDD	VDD rise rate to ensure internal Power-on Reset signal	0.05*	—	—	V/ms	See section on Power-on Reset for details
	IDD	Supply Current(2)					RC and XT osc configuration(4)
D010			—	1.8	4.5	mA	FOSC = 4.0 MHz, VDD = 5.5V
D010A			—	7.3	10	mA	FOSC = 4.0 MHz, VDD = 5.5V (During Flash programming)
							HS osc configuration (PIC16F84-10)
D013			—	5	10	mA	FOSC = 10 MHz, VDD = 5.5V
D020	IPD	Power-down Current(3)	—	7.0	28	µA	VDD = 4.0V, WDT enabled, industrial
D021			—	1.0	14	µA	VDD = 4.0V, WDT disabled, commercial
D021A			—	1.0	16	µA	VDD = 4.0V, WDT disabled, industrial

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as I/O pin loading and switching rate, oscillator type, internal code execution pattern, and temperature also have an impact on the current consumption.
The test conditions for all IDD measurements in active operation mode are:
OSC1=external square wave, from rail to rail; all I/O pins tristated, pulled to VDD, T0CKI = VDD, $\overline{MCLR}$ = VDD; WDT enabled/disabled as specified.

3: The power down current in SLEEP mode does not depend on the oscillator type. Power-down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD and VSS.

4: For RC osc configuration, current through Rext is not included. The current through the resistor can be estimated by the formula $I_R = V_{DD}/2R_{ext}$ (mA) with Rext in kOhm.

11.2 DC CHARACTERISTICS: PIC16LF84, PIC16LF83 (Commercial, Industrial)

DC Characteristics Power Supply Pins			Standard Operating Conditions (unless otherwise stated) Operating temperature 0°C ≤ TA ≤ +70°C (commercial) -40°C ≤ TA ≤ +85°C (industrial)				
Parameter No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
D001	VDD	Supply Voltage	2.0	—	6.0	V	XT, RC, and LP osc configuration
D002	VDR	RAM Data Retention Voltage(1)	1.5*	—	—	V	Device in SLEEP mode
D003	VPOR	VDD start voltage to ensure internal Power-on Reset signal	—	VSS	—	V	See section on Power-on Reset for details
D004	SVDD	VDD rise rate to ensure internal Power-on Reset signal	0.05*	—	—	V/ms	See section on Power-on Reset for details
	IDD	Supply Current(2)					RC and XT osc configuration(4)
D010			—	1	4	mA	FOSC = 2.0 MHz, VDD = 5.5V
D010A			—	7.3	10	mA	FOSC = 2.0 MHz, VDD = 5.5V (During Flash programming)
							LP osc configuration
D014			—	15	45	µA	FOSC = 32 kHz, VDD = 2.0V, WDT disabled
D020	IPD	Power-down Current(3)	—	3.0	16	µA	VDD = 2.0V, WDT enabled, industrial
D021			—	0.4	7.0	µA	VDD = 2.0V, WDT disabled, commercial
D021A			—	0.4	9.0	µA	VDD = 2.0V, WDT disabled, industrial

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as I/O pin loading and switching rate, oscillator type, internal code execution pattern, and temperature also have an impact on the current consumption.
The test conditions for all IDD measurements in active operation mode are:
OSC1=external square wave, from rail to rail; all I/O pins tristated, pulled to VDD, T0CKI = VDD, $\overline{MCLR}$ = VDD; WDT enabled/disabled as specified.

3: The power down current in SLEEP mode does not depend on the oscillator type. Power-down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD and VSS.

4: For RC osc configuration, current through Rext is not included. The current through the resistor can be estimated by the formula IR = VDD/2Rext (mA) with Rext in kOhm.

11.3 DC CHARACTERISTICS: PIC16F84, PIC16F83 (Commercial, Industrial) PIC16LF84, PIC16LF83 (Commercial, Industrial)

DC Characteristics All Pins Except Power Supply Pins			Standard Operating Conditions (unless otherwise stated) Operating temperature 0°C ≤ TA ≤ +70°C (commercial) -40°C ≤ TA ≤ +85°C (industrial) Operating voltage VDD range as described in DC spec Section 11.1 and Section 11.2.				
Parameter No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
	VIL	**Input Low Voltage** I/O ports					
D030		with TTL buffer	VSS	—	0.8	V	4.5 V ≤ VDD ≤ 5.5 V(4)
D030A			VSS	—	0.16VDD	V	entire range(4)
D031		with Schmitt Trigger buffer	VSS	—	0.2VDD	V	entire range
D032		MCLR, RA4/T0CKI	Vss	—	0.2VDD	V	
D033		OSC1 (XT, HS and LP modes)(1)	Vss	—	0.3VDD	V	
D034		OSC1 (RC mode)	Vss	—	0.1VDD	V	
	VIH	**Input High Voltage** I/O ports		—			
D040		with TTL buffer	2.4	—	VDD	V	4.5 V ≤ VDD ≤ 5.5V(4)
D040A			0.48VDD	—	VDD	V	entire range(4)
D041		with Schmitt Trigger buffer	0.45VDD	—	VDD		entire range
D042		MCLR, RA4/T0CKI, OSC1 (RC mode)	0.85 VDD	—	VDD	V	
D043		OSC1 (XT, HS and LP modes)(1)	0.7 VDD	—	VDD	V	
D050	VHYS	Hysteresis of Schmitt Trigger inputs	TBD	—	—	V	
D070	IPURB	PORTB weak pull-up current	50*	250*	400*	µA	VDD = 5.0V, VPIN = VSS
	IIL	**Input Leakage Current**(2,3) I/O ports	—	—	±1	µA	Vss ≤ VPIN ≤ VDD, Pin at hi-impedance
D061		MCLR, RA4/T0CKI	—	—	±5	µA	Vss ≤ VPIN ≤ VDD
D063		OSC1	—	—	±5	µA	Vss ≤ VPIN ≤ VDD, XT, HS and LP osc configuration
	VOL	**Output Low Voltage** I/O ports	—	—	0.6	V	IOL = 8.5 mA, VDD = 4.5V
D083		OSC2/CLKOUT	—	—	0.6	V	IOL = 1.6 mA, VDD = 4.5V
	VOH	**Output High Voltage** I/O ports(3)	VDD-0.7	—	—	V	IOH = -3.0 mA, VDD = 4.5V
D092		OSC2/CLKOUT	VDD-0.7	—	—	V	IOH = -1.3 mA, VDD = 4.5V

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: In RC oscillator configuration, the OSC1 pin is a Schmitt Trigger input. Do not drive the PIC16F8X with an external clock while the device is in RC mode, or chip damage may result.

2: The leakage current on the MCLR pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

3: Negative current is defined as coming out of the pin.

4: The user may choose the better of the two specs.

11.4 DC CHARACTERISTICS: PIC16F84, PIC16F83 (Commercial, Industrial) PIC16LF84, PIC16F83 (Commercial, Industrial)

DC Characteristics All Pins Except Power Supply Pins			Standard Operating Conditions (unless otherwise stated) Operating temperature 0°C ≤ TA ≤ +70°C (commercial) -40°C ≤ TA ≤ +85°C (industrial) Operating voltage VDD range as described in DC spec Section 11.1 and Section 11.2.				
Parameter No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
		Capacitive Loading Specs on Output Pins					
D100	COSC2	OSC2 pin	—	—	15	pF	In XT, HS and LP modes when external clock is used to drive OSC1.
D101	CIO	All I/O pins and OSC2 (RC mode)	—	—	50	pF	
		Data EEPROM Memory					
D120	ED	Endurance	1M	10M	—	E/W	25°C at 5V
D121	VDRW	VDD for read/write	VMIN	—	6.0	V	VMIN = Minimum operating voltage
D122	TDEW	Erase/Write cycle time	—	10	20*	ms	
		Program Flash Memory					
D130	EP	Endurance	100	1000	—	E/W	
D131	VPR	VDD for read	VMIN	—	6.0	V	VMIN = Minimum operating voltage
D132	VPEW	VDD for erase/write	4.5	—	5.5	V	
D133	TPEW	Erase/Write cycle time	—	10	—	ms	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

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